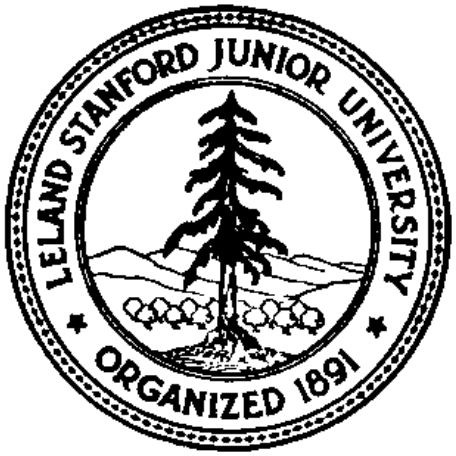
EE113 Course Notes
Electronic Circuits



Stanford University
Department of Electrical Engineering

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Chapter 1: INTRODUCTION

Minimalism is in, and there's nothing more minimal than nothing...
Barden N. Shimbo, Former EE122 Student

1: OBJECTIVES

• Get some *practical* knowledge about the design and analysis of basic analog circuits.

• Learn about operational amplifiers and circuits that use them.

• Find out how bipolar transistors *really* work in circuits.

• Learn how to design, analyze, and test basic amplifiers.

• Learn about differential pairs, current sources and multi-stage amplifier design.

• Learn how to design, analyze and test multi-stage amplifiers.

• Learn about feedback as it applies to amplifiers.

2: EE113 AND EE122 - A WINNING COMBINATION

To the extent possible, EE113 and EE122 are parallel courses. In general, the lectures, problem sets, and overall topics will be timed so that you will have the background knowledge to cope with the laboratories. The point is that (finally) you get to apply what you learn in the classroom to hands-on designing and testing of circuits. A potential problem arises if you don't keep up: you can be lost in two classes at once!

PLEASE DON'T GET LEFT BEHIND!!! IF YOU FEEL THIS HAPPENING, PLEASE LET US KNOW!

THE COURSES ARE ROUGHLY SYNCHRONIZED, BUT YOU WILL NEED TO READ AHEAD (TEXT AND NOTES) SOMETIMES!

3: COURSE INFORMATION

Instructor:	Prof. Greg Kovacs Office: CISX 202 Email: kovacs@cis Phone: 725-3637 **(email greatly preferred for setting up meetings)**
Lectures:	Skilling 193 Mon-Wed-Fri , 10:00am - 10:50 am
Office Hours: **(Subject to Change)**	Mon 11:00 am - 12:00 pm Wed 2:00 pm - 3:00 pm Fri 1:00 pm - 2:00 pm (Or by appointment please.)
Admin. Assistant:	Ms. Susan Kahn CISX 203 Phone: 723-0720 email: skahn@leland Hours: 10:00 am - 3:00 pm MTWTF
TA:	Nolan Sharp Email: nolans@leland Office Hours TBD Review Sessions TBD
Texts/Notes:	Sedra and Smith, “Microelectronic Circuits,” HRW Notes handed out in class + supplements as needed.
References:	Horowitz and Hill, “The Art of Electronics,” Cambridge Press Savant, Roden, and Carpenter, “Electronic Design,” Benjamin Cummings Gray and Meyer, “Analysis and Design of Analog Integrated Circuits,” 2nd Edition, Wiley Neudeck, “PN Junction Diodes,” and “The Bipolar Junction Transistor,” Addison-Wesley Muller and Kamins, “Device Electronics for Integrated Circuits,” 2nd Edition, Wiley

Credit: 3 units, letter grade only

Grading: **Homework** = 10% assigned weekly, due at 5pm on date marked on assignment in box at CISX 203. Please don't be late (penalties may apply).

Midterm Exam ± Quizzes = 35% **(OPEN BOOK)**

Final Exam = 55% **(OPEN BOOK)**

4: OUTLINE OF THE COURSE

INTRODUCTION AND REVIEW (handed out, but not covered in class)

BJT REVIEW (handed out, covered briefly in class if needed)

THE OPERATIONAL AMPLIFIER

COMMON EMITTER BJT AMPLIFIERS

GENERALIZED FREQUENCY RESPONSE ESTIMATION

COMMON BASE BJT AMPLIFIERS

COMMON COLLECTOR BJT AMPLIFIERS

CASCADED/CASCODED BJT AMPLIFIERS

DIFFERENTIAL AMPLIFIERS

CURRENT SOURCES

MULTI-STAGE AMPLIFIERS

FEEDBACK: THEORY AND PRACTICE

Analog Boot Camp Drill Routine

by G. Kovacs

(The words are first barked out by the professor, then shouted back by students marching in formation.)

Analog circuits sure are fine,
Just can't get 'em off my mind.

Digital circuits ain't my kind,
Zeros and ones for simple minds.

I guess NAND gates aren't all that bad,'
'Cause I need them for circuit CAD.

One, two, three, four,
Gain and bandwidth, we want more.

Five, six, seven, eight,
We don't want to oscillate.

Widlar, Wilson, Brokaw too,
They've got circuits, how 'bout you?

(repeat)

Chapter 2: BASIC CONCEPTS

I'm a bilingual illiterate...
I can't read or write in two languages.
Former EE113 Student

1: OBJECTIVES

• To review sources, signals, amplifiers, transfer functions, and Bode plots.

• To discuss noise, distortion and large versus small signals.

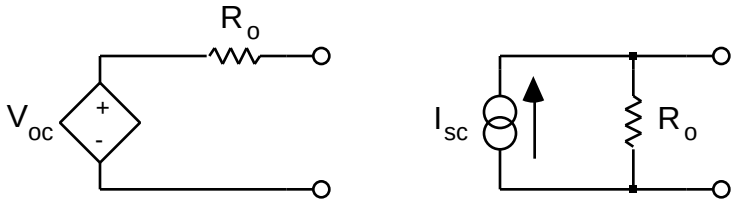
READING:

READ S&S Sections 1.1 - 1.5

READ APPENDIX E in S&S!!!

2: SOURCES

Thévenin & Norton $I_{SC} = \frac{V_{OC}}{R_o}$



You should review this briefly and know how to convert back and forth. The Norton form has a current source whose value is found by short-circuiting the Thévenin form. The Thévenin's voltage source is found by taking the open-circuit voltage of the Norton form. The output resistance, R_o, remains the same in both forms, but its orientation in the circuit changes.

3: SIGNALS

Fourier Series - a way to represent periodic signals as a sum of sine and cosine "harmonics"

$$x(t) = \sum_{n=0}^{\infty} \left\{ a_n \cos(n\omega_o t) + b_n \sin(n\omega_o t) \right\}$$

One can determine the fourier coefficients (a_n and b_n) using the following equations:

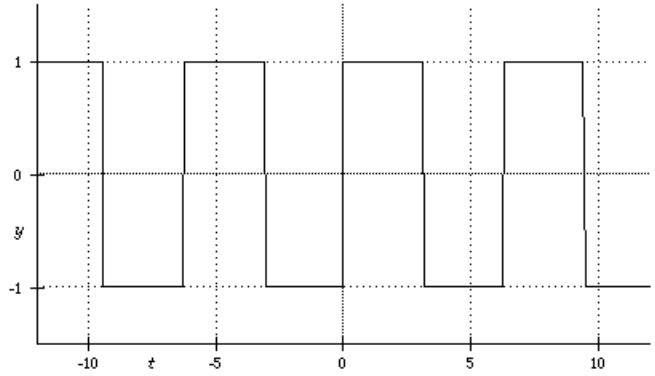
$$a_o = \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} x(t)\, dt$$ ← The DC term

$$a_n = \frac{2}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} x(t) \cos(n\omega_o t)\, dt$$ ← For Even Functions

$$b_n = \frac{2}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} x(t) \sin(n\omega_o t)\, dt$$ ← For Odd Functions

It is often useful to look at the function and decide if it's even or odd.

Example 1: symmetrical square wave (odd -> sine terms only)



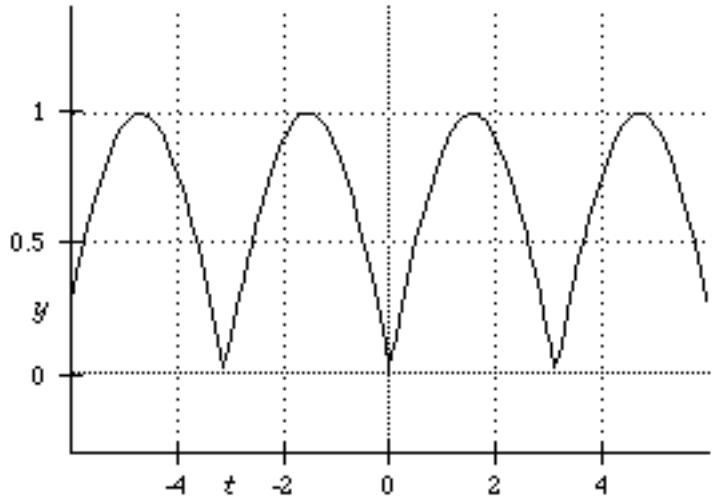
$$x(t) = \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \sin(n\omega_o t)$$

n's = 1,3,5... (odd)

b_n's = $\frac{4}{\pi}, \frac{4}{3\pi}, \frac{4}{5\pi}$ ...

(since the signal is odd, all a_n's are zero)

Example 2: Full Wave Rectified Sinewave. This is a common signal found in power supplies after the sinewave input power has been rectified using a diode or diodes and if an output filter capacitor is not used.



$$x(t) = \frac{2}{\pi} - \frac{4}{\pi} \sum_{n=2,4,6,...}^{\infty} \frac{\cos(n\omega_o t)}{n^2 - 1}$$

RMS Value of an AC signal - the amount of DC power required to provide an equivalent amount of heating in a resistive load... it is very useful when measuring the energy or power in signals that might not be a well-known waveform.

To compute the RMS, take the signal, square it, average it, and take the square root...

$$V_{RMS} = \sqrt{AVG\{v(t)^2\}} = \sqrt{\frac{1}{T}\int_0^T v^2(t)\,dt}$$

Some useful RMS formulas:

$$\text{Sinewave RMS} = \frac{V_{peak}}{\sqrt{2}} = \frac{V_{peak\text{-}to\text{-}peak}}{2\sqrt{2}}$$

$$\text{Symmetrical Squarewave RMS} = V_{peak} = \frac{V_{peak\text{-}to\text{-}peak}}{2}$$

$$\text{Triangle Wave RMS} = \frac{V_{peak}}{\sqrt{3}} = \frac{V_{peak\text{-}to\text{-}peak}}{2\sqrt{3}}$$

The AD536/AD636 AC/RMS Converter chip from Analog Devices directly computes the RMS value of an analog signal and it, or a close relative, is included in most hand-held digital multimeters.

4: AMPLIFIERS

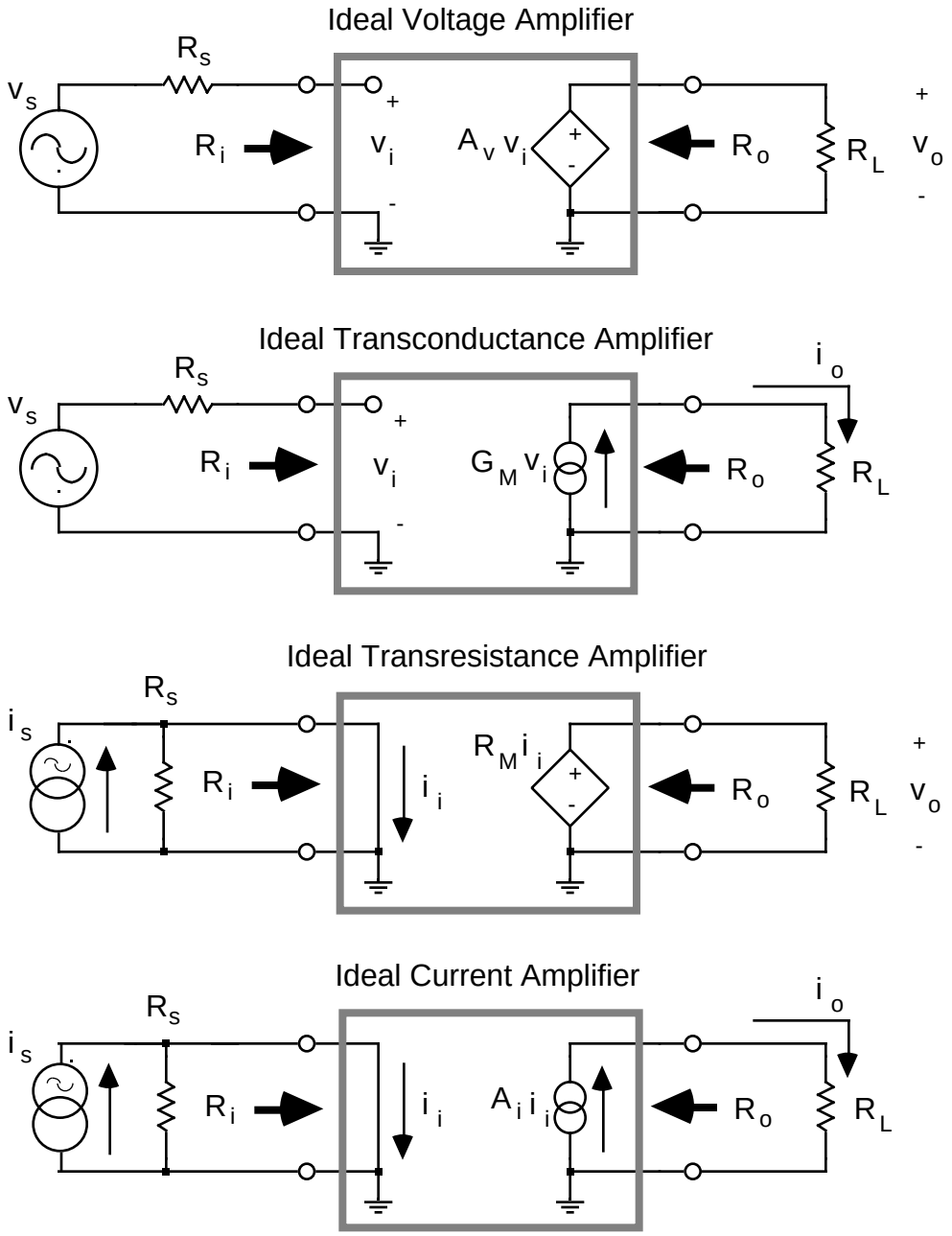
TYPES OF AMPLIFIERS

Amplifiers always increase (or at least maintain) the signal power. The gain of an amplifier is expressed as a voltage gain, transconductance gain (voltage input, current output), transresistance (current input, voltage output) or current gain. Thus, there are four basic types of amplifiers, depending on what it is that they amplify (voltage or current) and what it is that you want as their output (voltage or current).

One can model any amplifier as any of the four types, but the **intended use** of the amplifier usually makes one choice usually the best. In other words, an amplifier is usually *designed* to be a particular type.

Source Parameter to be Amplified	Desired Output Parameter	Type of Amplifier	Gain Expression
source voltage, v_s	v_o	Voltage	$A_v = \frac{v_o}{v_s}$ = voltage gain (dimensionless)
source voltage, v_s	i_o	Transconductance	$G_m = \frac{i_o}{v_s}$ = transconductance in Ω^{-1} or Siemens
source current, i_s	v_o	Transresistance	$R_m = \frac{v_o}{i_s}$ = transresistance in Ω
source current, i_s	i_o	Current	$A_i = \frac{i_o}{i_s}$ = current gain (dimensionless)

SCHEMATICS OF THE BASIC AMPLIFIER TYPES



NOTE 1: in general use Z (for impedance) rather than R, since most inputs and outputs are not purely resistive!

NOTE 2: R_S is shown as a resistor at the input of the amplifier that effectively attenuates the input signal if the amplifier is not ideal (i.e. if the voltage input amplifiers have input resistances less than infinity or if the current input amplifiers have input resistances greater than zero).

Type of Amplifier	Gain Expression	Ideal Input Impedance	Ideal Output Impedance
Voltage	$A_v = \frac{v_o}{v_s}$ = voltage gain (dimensionless)	$Z_i = \infty$	$Z_o = 0$
Transconductance	$G_m = \frac{i_o}{v_s}$ = transconductance in Ω^{-1} or Siemens	$Z_i = \infty$	$Z_o = \infty$
Transresistance	$R_m = \frac{v_o}{i_s}$ = transresistance in Ω	$Z_i = 0$	$Z_o = 0$
Current	$A_i = \frac{i_o}{i_s}$ = current gain (dimensionless)	$Z_i = 0$	$Z_o = \infty$

BASIC AMPLIFIER SPECIFICATIONS

• **GAIN** is usually expressed in *decibels* in terms of the input and output parameters:

$$\text{VOLTAGE GAIN} = A_v = \frac{v_o}{v_i}$$

• Decibels (after Alexander Graham Bell) are a common unit of measure. POWER gain is expressed as:

$$dB = 20 \log_{10}(A_v)$$

NOTE! if the input and output signals are already POWER, then use,

$$dB = 10 \log_{10}\left(\frac{P_{out}}{P_{in}}\right) dB = 20 \log_{10}(A_v)$$

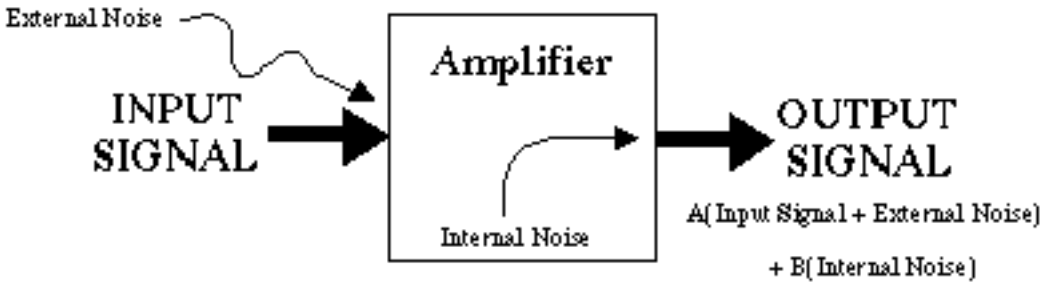
$$\text{POWER GAIN} = A_p = \frac{p_o}{p_i} = \frac{i_o v_o}{i_i v_i}$$

When calculating the overall gain of a cascaded amplifier, simply **add** up the gain (or loss) of each stage in dB to get the overall gain.

5: NOISE

• **NOISE** is unwanted signal(s) that end up added to the desired signals.

• Noise can originate outside of an amplifier or come from inside of the amplifier.



• **Interference** -> electromagnetic interference (EMI) is "picked-up" signals from **external** noise sources such as household wiring, automobile ignitions, etc.

SOLUTION = shielding!

• **Thermal Noise** -> noise from random motion of electrons in conductors (proportional to temperature) -> if the conductor is a resistor, the higher its value, the more noise **voltage** is generated (thermal noise is also a function of the signal bandwidth).

$$v_n(\mathrm{RMS}) = \sqrt{4kTR\Delta f}$$

where k is Boltzmann's constant (1.38 X 10^{-23} J/°K), T is the absolute temperature in °K, R is the component's resistance in Ω, and Δf is the bandwidth of interest in Hz.

SOLUTION = use low-resistance values or cool your circuit

• **Shot Noise** -> noise **current** that occurs in active semiconductor devices (BJT's, FET's, etc.) due to the arrival and departure of individual carriers in the device...

$$i_n(\mathrm{RMS}) = \sqrt{2eI\Delta f}$$

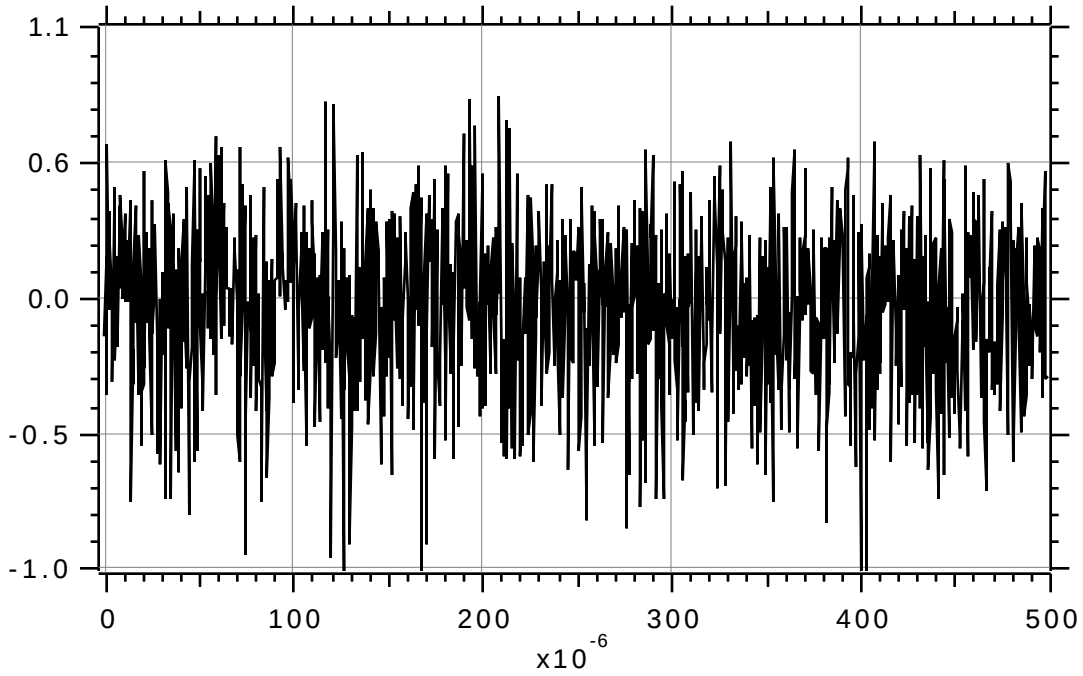
where e is the charge on the electron (1.6 X 10^{-19} C), I is the DC current flowing, and Δf is the bandwidth of interest in Hz. This is proportional to the current.

SOLUTION = use lower currents.

• **Flicker Noise** -> low-frequency noise (1/f dependence of frequency spectrum) generated by the random recombination of electrons and holes in semiconductors, or by fluctuations in component values, generally only containing frequencies in the audio spectrum (bad for stereo gear!).

SOLUTION = move to another universe.

• **“White” noise** is noise that has a flat frequency spectrum (i.e. contains all frequencies in equal proportion). In practice, noise is only “white” over a finite bandwidth. The sound from an FM receiver between channels is more-or-less white.



An actual "white noise" signal with bandwidth limited to 20 kHz.

• White noise can be really useful for determining the frequency response of circuits using a spectrum analyzer - all frequencies are equally represented in the spectrum of white noise, so you can input it into a circuit you are testing and look at which frequencies come out! If you average over a long enough time, you can obtain a frequency response for the circuit under test.

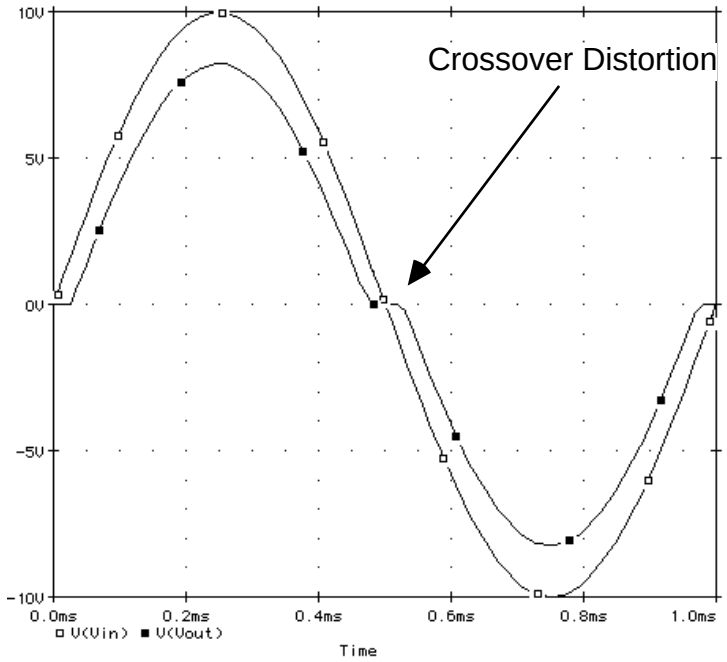
6: DISTORTION

• **DISTORTION** of a signal occurs when the amplified version of the signal coming out of the amplifier is not simply a scaled copy of the input signal, but is differently shaped (distorted).

• Distortion can be noted as a difference in waveform shape the ideal scaled copy of the input, a difference in the spectrum of the input and output signals, or sometimes observed by listening to the output of an amplifier (if it is used for audio).

• Distortion is due to nonlinearities, generally because the semiconductor (or tube) amplifier are not perfectly linear. In some cases, distortion can come from amplifier saturation ("clipping," or the amplifier simply reaching one of the voltage or current extremes beyond which it cannot swing).

• Another common type of distortion in amplifiers that use both PNP and NPN transistors at their outputs is ***crossover distortion***, which is caused by the slight "gap" in voltage between one type of transistor turning off and the other turning on.



• You can test for distortion by using a pure (single frequency) sinusoidal input signal and looking at the output either visually or with a spectrum analyzer. A linear system will only have the same frequency at its output. Nonlinearities will give rise to harmonics (signals at frequencies other than the one input to the system) which are measurable with the spectrum analyzer (and sometimes by your eye on an oscilloscope screen).

• The term ***total harmonic distortion*** (THD) represents the percentage of the total output signal of an amplifier that is at frequencies other than the one put in... in other words, you drive the amplifier with a pure sinewave at a frequency f_o and make a ratio of the power in the harmonics (i.e. sum of signal frequencies other than f_o, with amplitudes given by $A_i(f_i)$) to the input signal power.

$$\%\mathrm{THD} = \frac{\sum_{i=1}^{\infty} A_i(f_i)}{A_o(f_o)} \times 100\%$$

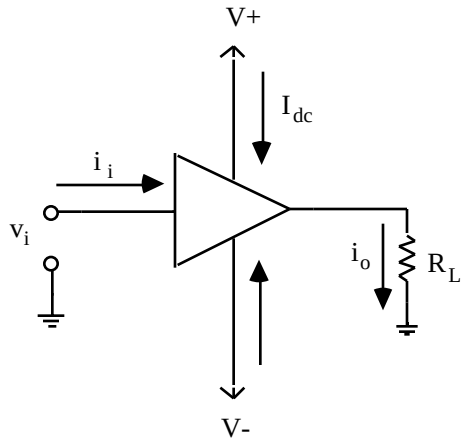
• In practice, one does not add up harmonic amplitudes to infinite frequency, but through the range of interest (e.g. up through 20 kHz for audio).

• Other amplifier specifications such as frequency response (bandwidth), gain, etc., will be discussed below.

7: AMPLIFIER POWER SUPPLIES & EFFICIENCY

• All amplifiers need some type of power supply to supply the extra energy that is delivered to the load.

• Most analog amplifiers use two power supply voltages or “rails,” as shown below,



• Some amplifiers use only a single power supply voltage, but sometimes they internally "split" that single voltage into two rails by making an artificial "ground" voltage half way from "real ground" to the supply voltage.

• The efficiency of an amplifier reflects the amount of power delivered to the load as a fraction of the total power drawn from the power supply, and can be computed using:

$$\eta = \frac{P_L}{P_{dc}} \times 100\% = \frac{\text{Power Delivered to Load}}{\text{Power Used from Power Supplies}} \times 100\%$$

8: LARGE AND SMALL SIGNALS

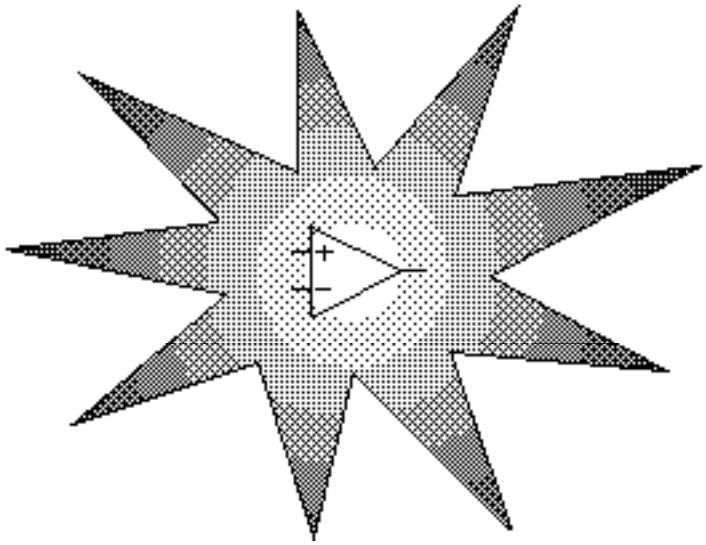
• ***Most circuits are linear if the input signals are small enough!*** If the signal amplitude is increased enough some type of nonlinearity will make itself obvious! All semiconductor devices (and vacuum tubes!) are very nonlinear, and the only reason we get nice, clean amplifier outputs is that we are keeping signal swings small enough through various techniques.

• Examples of ***large signal*** effects (as discussed above in "Distortion"):

• Amplifier **clipping** (saturation) -> here you have a case where the amplifier's output cannot swing above and below certain maximum and minimum voltages (that makes sense)... you have probably heard clipping when someone turned up a stereo too loud!

• Amplifier distortion due to transistor nonlinearities -> this is simplest to understand by considering that basically, all transistors are nonlinear devices and we work very hard to "coax" linearity out of them over certain ranges of signal level... this type of distortion can be minimized but can never be completely avoided.

• Amplifier exploding (very nonlinear) due to extremely large input signal:



When we talk about transfer functions, AC small-signal equivalent models, Bode plots, etc., we are always assuming that the circuit is in small-signal operation!

9: TRANSFER FUNCTIONS

• You already know what these are if you have ever looked at stereo equipment catalogs or specification sheets, since they are plotted to illustrate the frequency range over which the amplifier will operate properly.

• Amplifiers are either DC or AC coupled, meaning that the inputs are sensitive to both DC and AC signals ("DC-coupled") or only AC signals ("AC-coupled). You should note that oscilloscope amplifiers always have the option of choosing one or the other coupling modes.

• You can use capacitors at the inputs and outputs of amplifiers to “block” DC signals, as long as they are large enough to "look like shorts" in the frequency range of interest... This type of amplifier is called AC- or capacitively-coupled.

• The frequency response of such an AC-coupled circuit **cannot** extend to zero Hz.

• Here is a brief complex number review for your reference so you can compute transfer functions of circuits:

$$V = Re + jIm = A\,e^{j\theta}$$

$$Re = A\cos(\theta)$$

$$Im = A\sin(\theta)$$

$$|V| = \sqrt{Re^2 + Im^2}$$

$$\theta = \arctan\left(\frac{Im}{Re}\right)$$

Remember that $s = \sigma + j\,\omega$

POLES & ZEROS -> WHAT DO THEY MEAN?

Transfer Function Notation:

$$T(s) = \frac{v_{out}(s)}{v_{in}(s)} = A_o \frac{(s - z_1)(s - z_2)\cdots(s - z_N)}{(s - p_1)(s - p_2)\cdots(s - p_M)}$$

z_1 through z_N are the “zeros,” or the complex frequencies at which the numerator becomes zero (the transfer function goes to zero)...

p_1 through p_M are the “poles,” or the complex frequencies at which the denominator becomes zero (the transfer function goes to infinity)...

• The "order" of the system = N + M

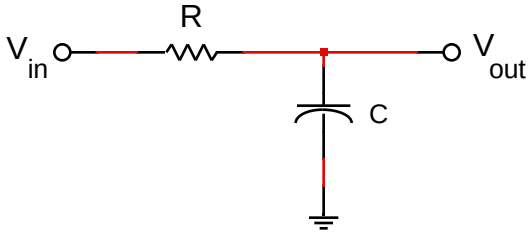
• A **zero** alone would make the output amplitude of a circuit i**ncrease forever** with increasing frequency. In real circuits, one cannot have a zero without a pole to "cancel" it out at some frequency.

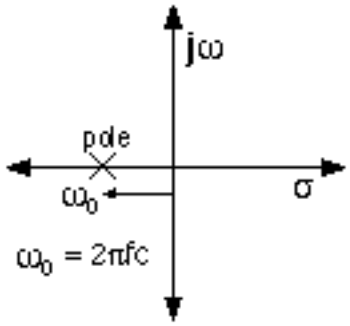
SIMPLE FILTERS

• The *cutoff (or 3dB) frequency* is the point at which the response is 3 dB lower than in the passband (≈ 0.707 times the passband amplitude).

HERE IS A GOOD IDEA TO GET A SENSE FOR CIRCUIT BEHAVIOR: Look at the circuit first before doing any math! The capacitors are all infinite impedance for DC and their impedance decreases toward zero as the frequency increases.

FIRST-ORDER RC LOW-PASS FILTER:





$$H(s) = \frac{\frac{1}{Cs}}{R + \frac{1}{Cs}} = \frac{1}{RCs + 1} = \frac{1}{1 + \frac{s}{\omega_o}}$$

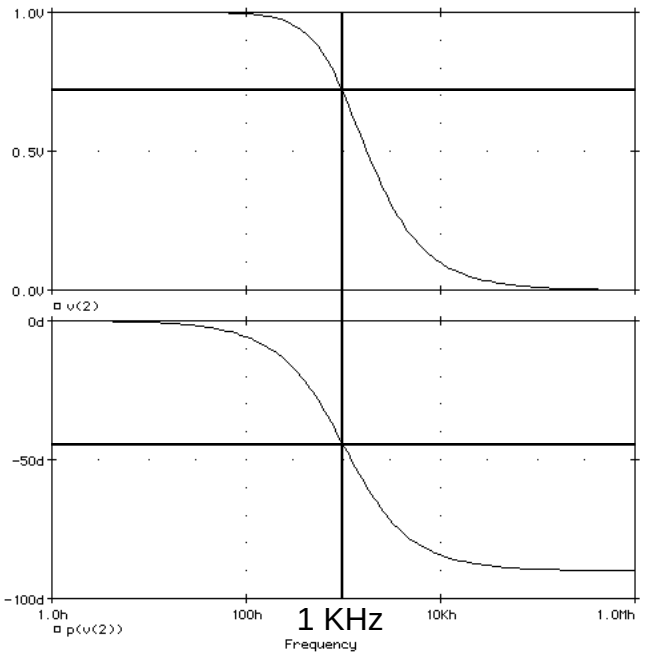
• The general form is $H(s) = \frac{K}{1 + \frac{s}{\omega_o}}$ OR $\frac{K\omega_o}{\omega_o + s} = \frac{A}{\omega_o + s}$

where K is the gain for low frequencies and $A = K\omega_o$

• The pole is at $S = -\omega_o$

• The "cutoff" frequency is at $\omega_0 = 2\pi f_c = \frac{1}{RC}$

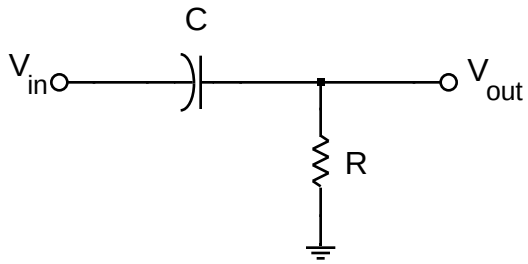
Gain and phase responses of the first-order, RC low-pass filter:

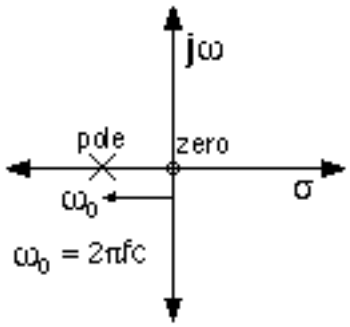


0.707 V

- 45°

FIRST-ORDER RC HIGH-PASS FILTER:





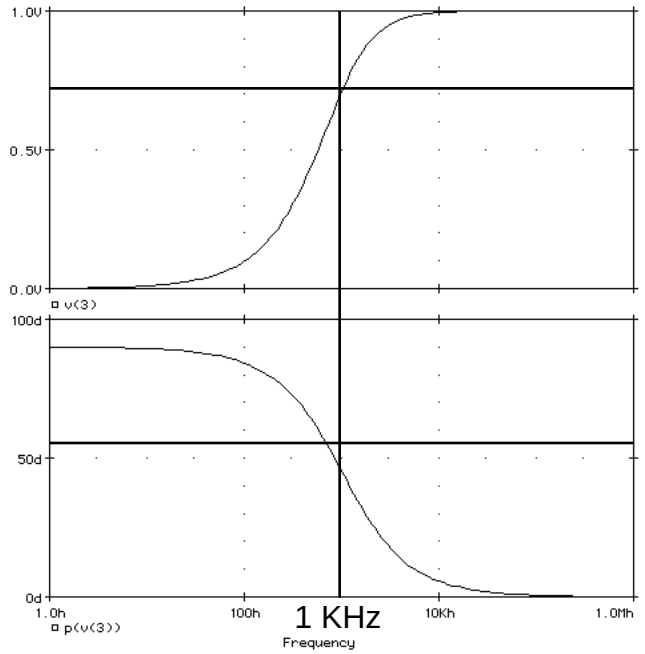
$$H(s) = \frac{R}{R + \frac{1}{Cs}} = \frac{RCs}{RCs + 1} = \frac{s}{s + \frac{1}{RC}} = \frac{s}{s + \omega_o}$$

• The general form is $\boxed{H(s) = \frac{Ks}{s + \omega_o}}$ where K is the gain for high frequencies

• The pole is at S = $-\omega_o$ and the zero is at S = 0

• The cutoff frequency is the same as for the low-pass filter.

Gain and phase responses of the first-order, RC high-pass filter:



10: BODE PLOTS

This material is covered in the prerequisites to EE113, but **typically, people are a bit "shaky" on phase plots**. The key point is that the **effect** of poles or zeros **starts to take place a decade before or a decade after the pole or zero frequency** when you are dealing with phase (unlike **at** the frequency for gain plots)!

If you are already familiar with all of this, you can skip to the next section.

THE BASIC IDEA:

The point is to be able to draw a "quick" sketch of a transfer function of a circuit.

It is **assumed that you have an equation** for the transfer function.

This is an **important technique**, despite the availability of computers!

You will need to be able to do Bode plots on exams and in some "real world" situations.

Remember that you can use computer programs like Matlab™, Mathematica™, Theorist™, etc. to check your work!

ADD up the individual responses of all of the poles and zeros of the transfer function. They each affect the frequency response “only” after they take effect at their respective “break” frequencies....

• a **pole** makes the amplitude **fall** with frequency by 20 dB /decade and “has no effect” before its break frequency

• a **zero** makes the amplitude **rise** with frequency by 20 dB/decade and “has no effect” before its break frequency

• a **pole** causes the phase to **fall** from 0° to -90° over two decades of frequency ***starting one decade before the break frequency*** -> the phase is -45° at its break frequency

• a **zero** causes the phase to **rise** from 0° to +90° over two decades of frequency ***starting one decade before the break frequency*** -> the phase is +45° at its break frequency

• **the effects of poles or zeros at “zero” frequency have already “maxed out” by the time you start your plot** (i.e. phase is -90° for a pole at zero frequency, and +90° for a zero at zero frequency)

HOW TO MAKE A GAIN PLOT

1) Write the transfer function equation in a form **so that you can see the break frequencies** of the poles and zeros.

2) Try to begin the sketch at a frequency where you **know the gain** (from looking at the equation).

If it is not obvious, draw a rough draft of the curve and select the frequencies corresponding to the "flat" parts, plug those frequencies in for "S", estimate the gain and convert to dB.

Remember about poles and/or zeros that may have already “taken effect” at low enough frequencies that they are “maxed out” before you start your sketch.

3) For each **zero**, add a **+20 dB/decade slope** to the slope of the sketch at the break frequency of that zero.

4) For each **pole**, add a **-20 dB/decade slope** to the slope of the sketch at the break frequency of that pole.

5) Draw a “smooth” curve over the sketch (the curves differ by about 3 dB at each single break)...

HOW TO MAKE A PHASE PLOT

1) Write the transfer function equation in a form **so that you can see the break frequencies** of the poles and zeros.

2) Try to begin the sketch at a frequency where you know the phase (from looking at the equation).

Remember about poles and/or zeros that may have already “taken effect” at low enough frequencies that they are “maxed out” before you start your sketch.

One way to make it easier is to start out assuming 0° at "super low" frequencies, then shift the whole phase sketch:

a) + 90° for any zeros at "zero frequency"

b) - 90° for any poles at "zero frequency"

c) +/- 180° if there is a negative sign

Remember that a negative sign on a gain is a 180° phase shift!

3) Each **zero** contributes a phase slope of **+45° per decade starting one decade below and lasting through one decade above** the break frequency.

The phase contribution from that zero is "half way there" (or contributing +45°) at the break frequency.

The contribution of that zero to phase at frequencies less that one tenth of the break frequency and greater than ten times the break frequency is zero!

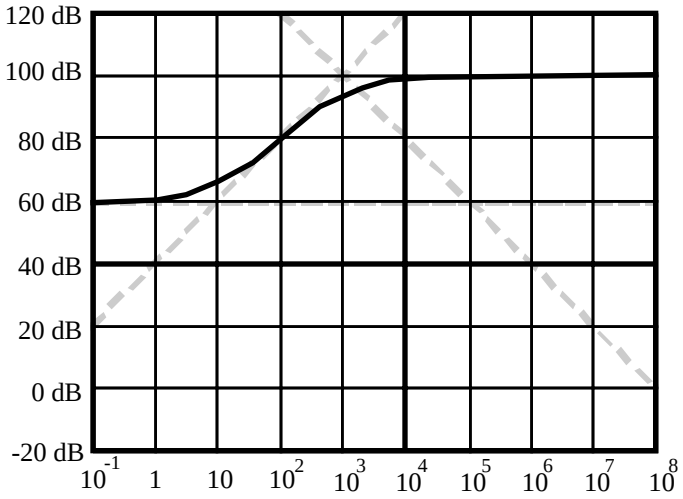
4) Each **pole** contributes a phase slope of **-45° per decade starting one decade below and lasting through one decade above** the break frequency.

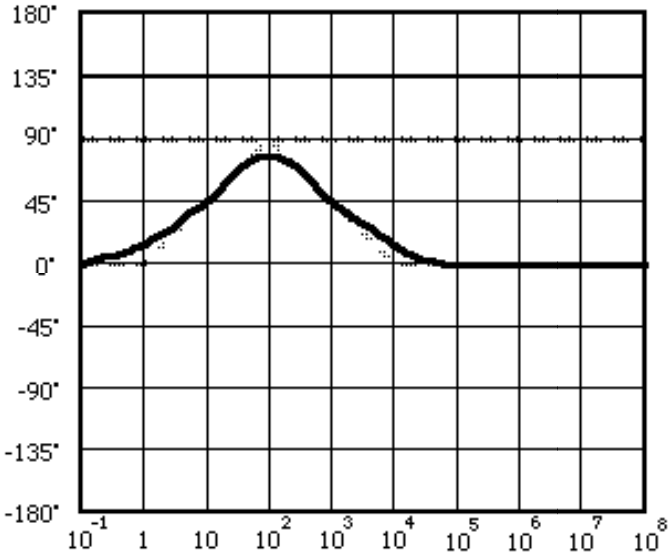
The phase contribution from that pole is "half way there" (or contributing -45°) at the break frequency.

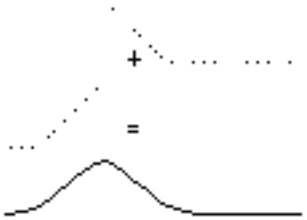
The contribution of that pole to phase at frequencies less that one tenth of the break frequency and greater than ten times the break frequency is zero!

5) Draw a "smooth" curve over the sketch (the curves differ by about 6° at each single break).

EXAMPLE 1: $H(s) = \dfrac{10^5(s + 10)}{(s + 10^3)}$







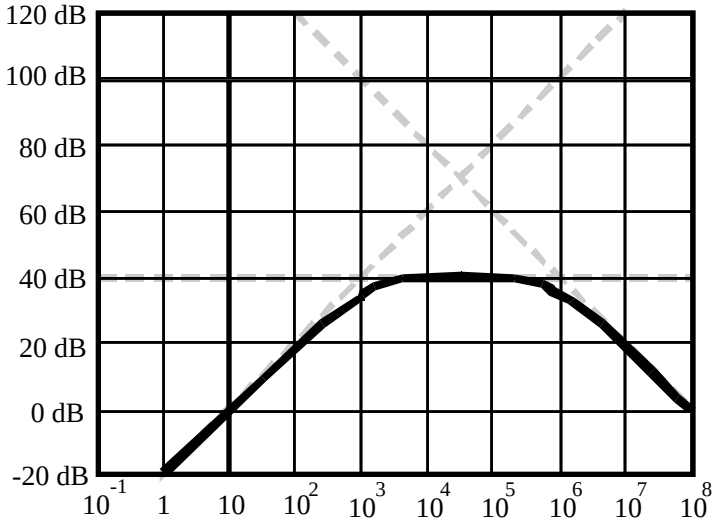
EXAMPLE 2: Typical Capacitor-Coupled Amplifier

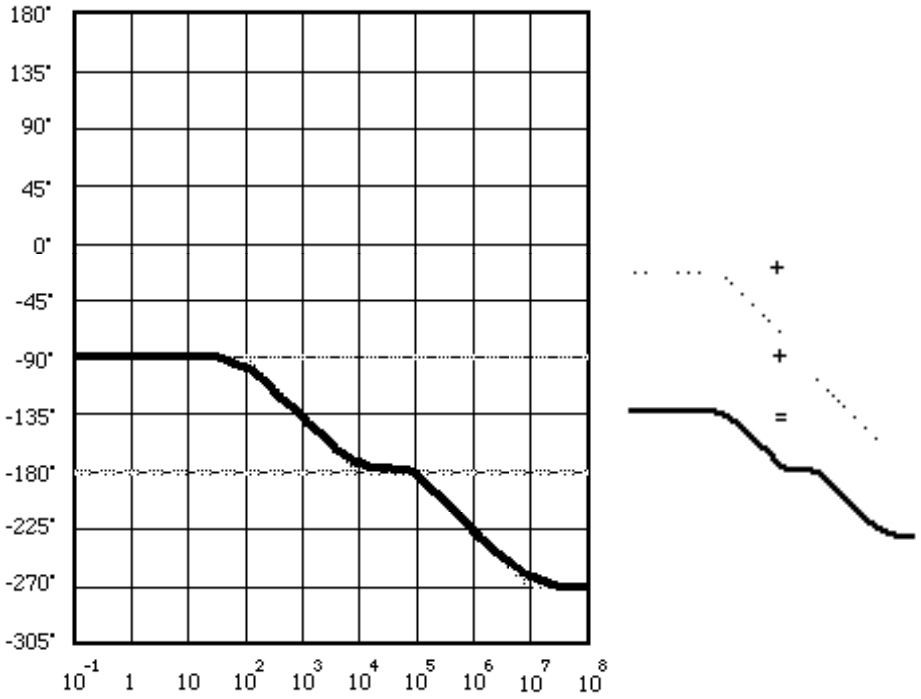
$$H(s) = -100\,\frac{s}{(s + 10^3)}\,\frac{1}{\left(1 + \dfrac{s}{10^6}\right)} = \frac{-10^8 s}{(s + 10^3)(s + 10^6)}$$

Here we have a zero at zero ('maxed out" by the time you start your plot), a pole at 10^3 radians/S and a pole at 10^6 radians/S.

In the midband, the first pole will have "cancelled" the zero and the gain should be flat at 100...

Below the first pole frequency, you should only need to consider the zero...





Chapter 3: BJT REVIEW

Without bipolar transistors, the world would be a pretty dull place!
Shockley, Bardeen and Brattain, Inventors of the bipolar transistor (they didn't really say it).

1: OBJECTIVES

BJT operation

BJT DC Analysis and DC Load Lines

BJT small-signal model -> hybrid π

Looking "in" each terminal

AC Load Lines

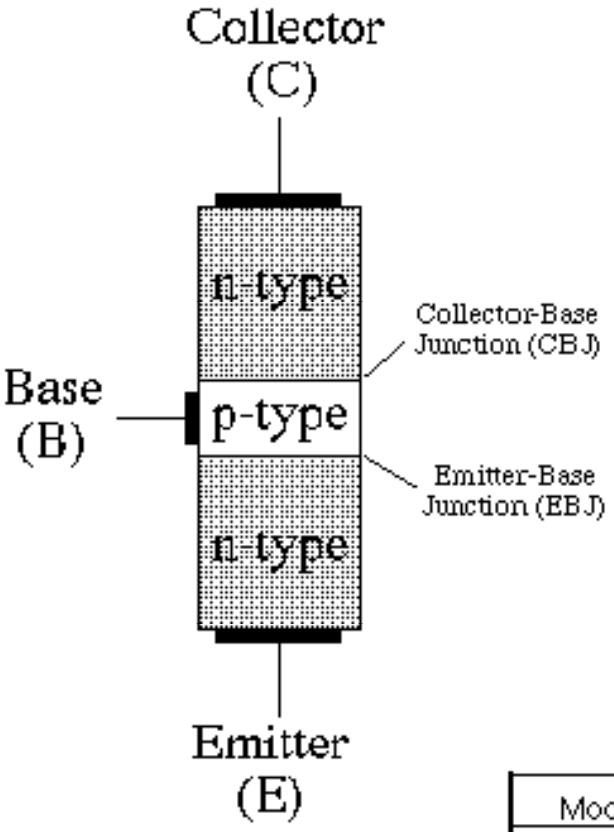
READ S&S Chapter 4, Sections 4.1 - 4.9

2: TYPES OF BIPOLAR JUNCTION TRANSISTORS

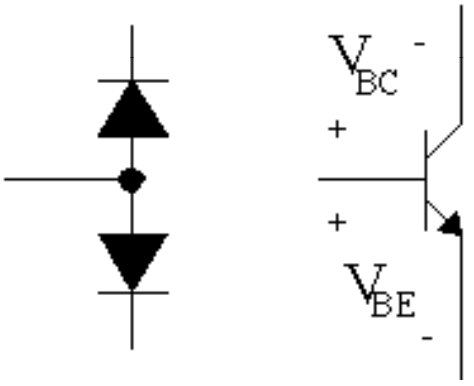
• There are two polarities: NPN ("not pointin' in") and PNP ("pointin' in"), where the "pointin'" part refers to the direction of the arrow on the emitter terminal.

• BJT's can operate as amplifiers (active mode) or switches (saturation = "ON," cutoff = "OFF")

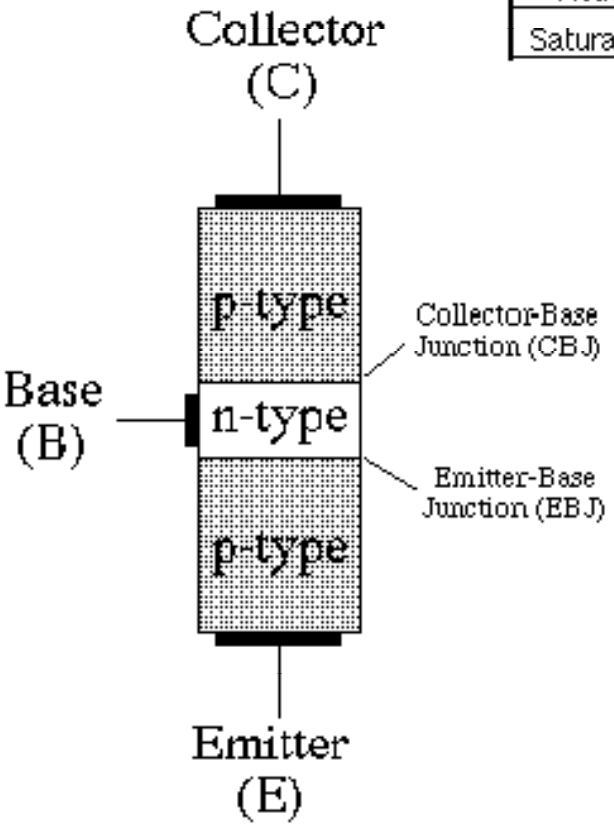
Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

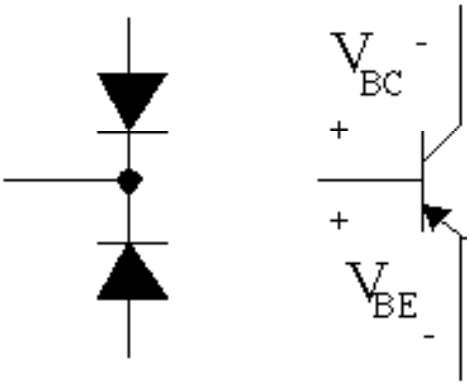


NPN



Mode	EBJ	CBJ.
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward





PNP

3: DC ANALYSIS (LARGE-SIGNAL)

• The collector current versus V_{BE} for a BJT is given by,

$$I_C = I_S\left(e^{\frac{qV_{BE}}{kT}} - e^{\frac{qV_{BC}}{kT}}\right)$$

$$I_B = \frac{I_S}{\beta_F}\left(e^{\frac{qV_{BE}}{kT}} - 1\right) + \frac{I_S}{\beta_R}\left(e^{\frac{qV_{BC}}{kT}} - 1\right)$$

where, in the lower equation, the forward current gain, β_F and the reverse current gain, β_R are considered to account for all possible operating modes. Generally, as seen below, we only use "β" and assume we are talking about β_F.

• For normal operation (assuming NPN), $V_{BE} > 0$ and $V_{BC} < 0$ so one can neglect the second exponential terms in both equations.

• I_S is the “current scale factor” which depends on the size of the transistor (in particular, the geometrical area of its emitter) and the process by which it was made.

• If it is **certain** that $V_{BC} < 0$ (base-collector junction is **reverse** biased) then one can use simplified forms of the above equations, simply neglecting the β_R terms and substituting the generic β for β_F.

$$I_C = I_S\, e^{\frac{qV_{BE}}{kT}} = I_S\, e^{\frac{V_{BE}}{V_T}}$$

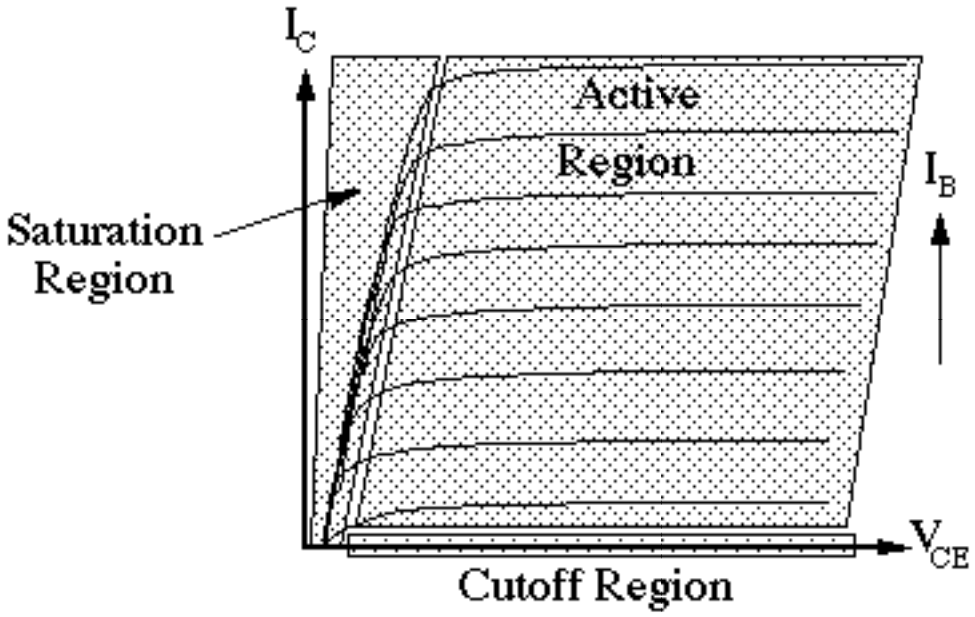
I_S may be on the order of 10^{-14} to 10^{-15}A

$$I_B = \frac{I_C}{\beta}$$

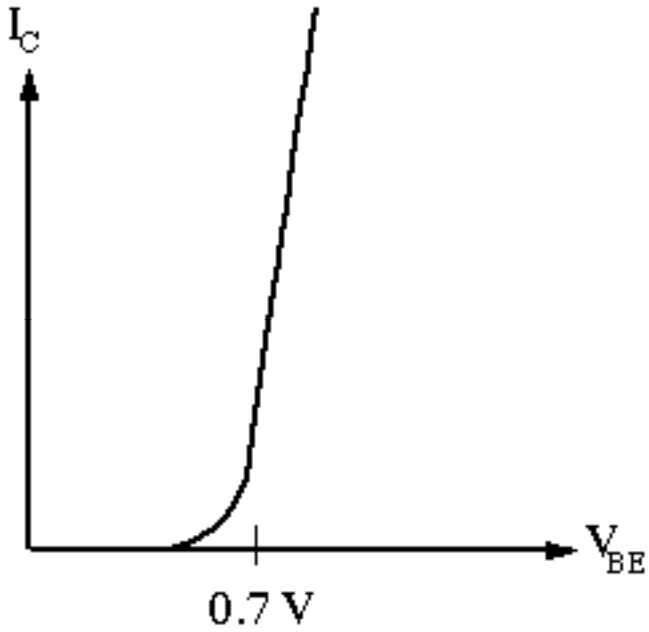
where kT/q ≈ 26 mV at room temperature.

• Another essential equation relates the emitter current to the base current:

$$I_E = I_C + I_B = (1+\beta)I_B \approx \beta I_B \quad \text{if } \beta \text{ is large!}$$



• The plot above shows the three regions of BJT operation: **active** (where analog amplifiers typically operate), **saturation** (when the transistor is "fully on") and **cutoff** (where the transistor is "fully off").



• The plot above shows the exponential relationship between I_C and V_{BE}... the point is that ***tiny*** changes in V_{BE} cause ***huge*** changes in I_C.

• Note that I_B vs. V_{BE} curve is just a scaled copy of the I_C vs. V_{BE} curve.

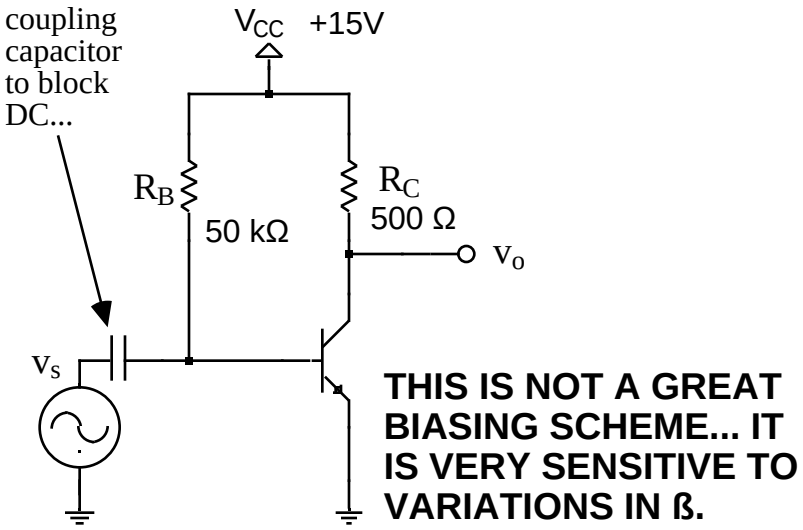
4: ANALYSIS OF BIASING

(Be careful... NPN & PNP are different for DC biasing! Here we look at NPN's)

1) Typically, you start out assuming that the base-emitter junction is forward biased (but later should verify that!)... $V_{BE} \approx +0.7V$

2) Check that the base-collector junction is reverse biased: $V_{BC} < 0$ (i.e. if so, then the transistor is not saturated). If $V_{BC} < 0$ and if I_B is uniquely determined, then $I_C = \beta I_B$

In practice, we generally assume that a transistor is not fully saturated until $V_{CE} \approx 0.2V$... this means that V_{BC} can be as much above zero as 0.5V before "full" saturation (see the curves above), but we really don't want to cut it that close for a real amplifier because the I_C vs V_{CE} curves start to really bend there, leading to distortion .



• Assume ß = 100...

• Start out assuming active mode, so $V_{BE} = 0.7V$.

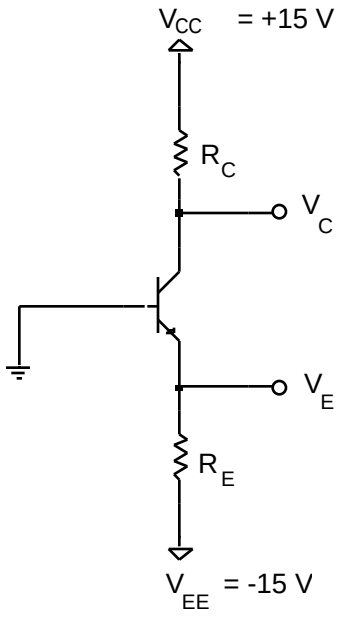
$$I_B = \frac{15 - 0.7}{50\text{k}\Omega} = 0.286 \text{ mA}$$

$$I_C = 100 I_B = 28.6 \text{ mA}$$

$$V_{CE} = 15\text{V} - (28.6 \text{ mA})(500\ \Omega) = 0.7 \text{ V}$$

• This means that the base-collector junction is at zero volts (on the edge between reverse and forward biased, but still not "on")... this means that the input signal would not have to swing very far to put the transistor into saturation (not good for an amplifier!).

• What if β > 100? For example, if β = 200, $V_{BC} > 0$!!! We don't want a forward biased BC junction...



$R_C = 1K\Omega \qquad R_E = 1K\Omega \qquad \beta_F = 100$

$V_E = -0.7\ V \qquad I_E = \dfrac{-0.7 - (-15V)}{1K} = 14.3mA$

$I_C = 14.3mA \left(\dfrac{\beta}{\beta + 1}\right) = 14.3mA \left(\dfrac{100}{101}\right) = 14.16mA$

$V_C = 15V - (14.16mA)\ 1K = 0.84V$

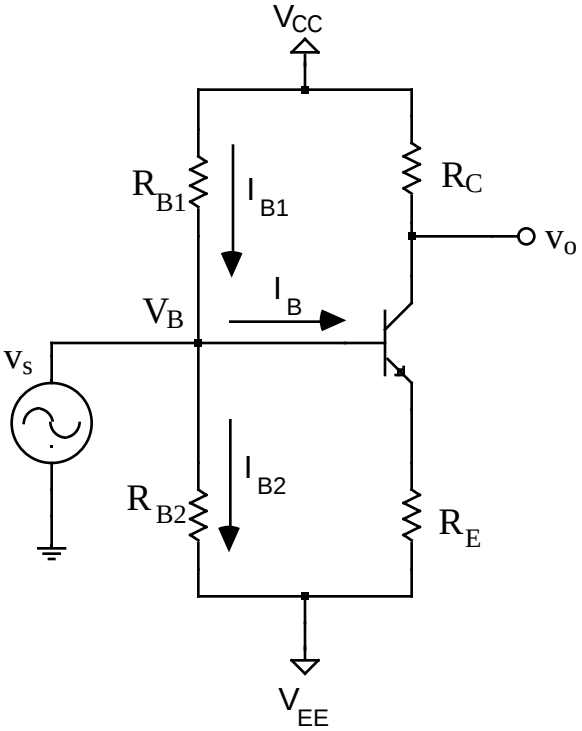
$V_{CE} =$ _____

$V_{BC} =$ _____

• The answers are: V_{CE} = 0.84 - (-0.7) = 1.54V (not saturated) and V_{BC} = 0 - 0.84 = -0.84 (reverse biased).

• What if ß is 200 now?... not much happens -> this is better biasing!

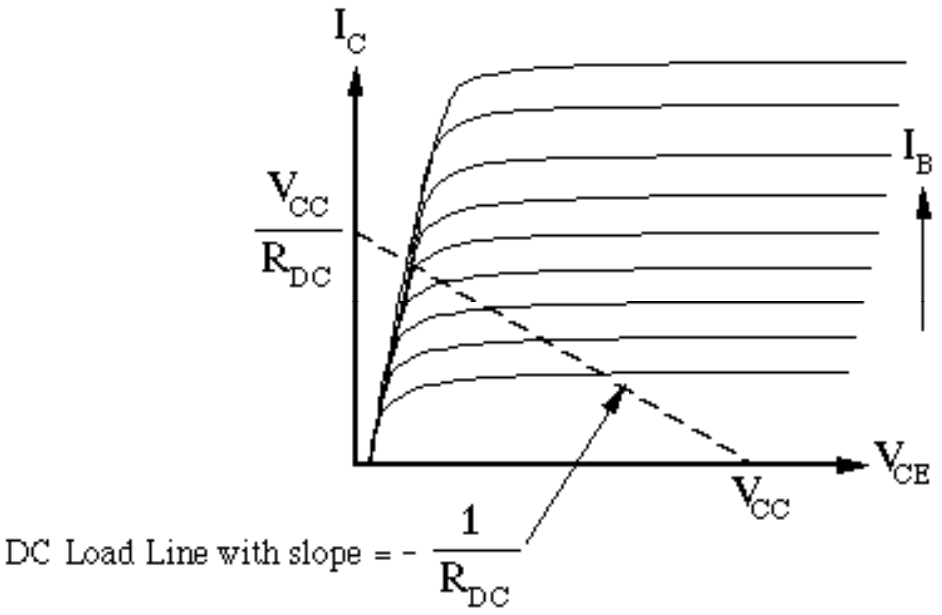
A MORE REALISTIC BIAS CIRCUIT (COVERED IN THE CE AMPLIFIER SECTION):



5: DC LOAD LINES

• This is a graphical approach to solving two simultaneous equations: the current vs. voltage characteristic of the resistor in the collector circuit (just Ohm's Law) and the I_C vs V_{CE} characteristic of the transistor (for a given base current).

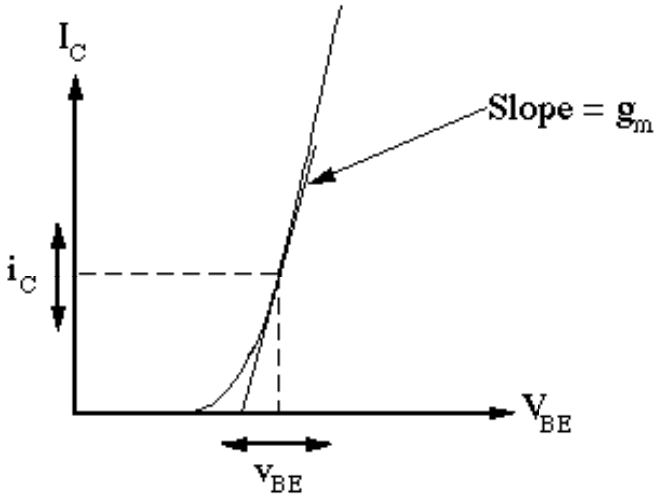
• The intersection of the two current vs. voltage curves is the quiescent point ("Q-point"), which is where the amplifier "idles" with no AC input signal.



6: SMALL-SIGNAL BEHAVIOR

• The goal when modeling small-signal behavior is to make a model of a the transistor that works for signals small enough to "keep things linear" (i.e. not distort too much).

• The basic trick is to linearize the very nonlinear exponential relationship between V_{BE} and I_C by looking at a small enough region of the exponential... The transistor's behavior is almost linear if the region is quite small...



$$I_C + i_c = I'_C = I_S\, e^{\frac{(V_{BE} + v_{be})}{V_T}} \qquad \text{DC + AC current}$$

$$= \left(I_S\, e^{\frac{qV_{BE}}{kT}}\right)\left(e^{\frac{v_{be}}{V_T}}\right)$$

$$= I_C \left(e^{\frac{v_{be}}{V_T}}\right)$$

$$= I_C \left(1 + \frac{v_{be}}{V_T} + \ldots\right) \qquad \text{expand....}$$

$$I'_C = I_C + \frac{I_C}{V_T}\, v_{be} = I_C + g_m\, v_{be} \qquad \text{linearize...}$$

This assumes $v_{be} << \frac{kT}{q} = V_T \approx 25.9\ \text{mV}$

$g_m \equiv \frac{I_C}{V_T}$ THE TRANSCONDUCTANCE

• Now one can look at i_b versus v_{be}... want to look at it as an equivalent input resistance, r_π, that models the input of the transistor for small signals.

• The AC component of the collector current from above is,

$$i_c = g_m v_{be}$$

and

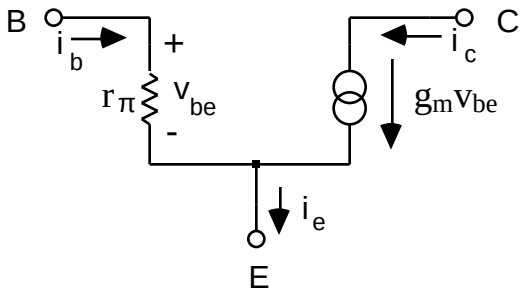
$$i_c = \beta i_b$$

therefore,

$$\beta i_b = g_m v_{be} \quad \rightarrow \quad \boxed{r_\pi = \frac{v_{be}}{i_b} = \frac{\beta}{g_m}}$$

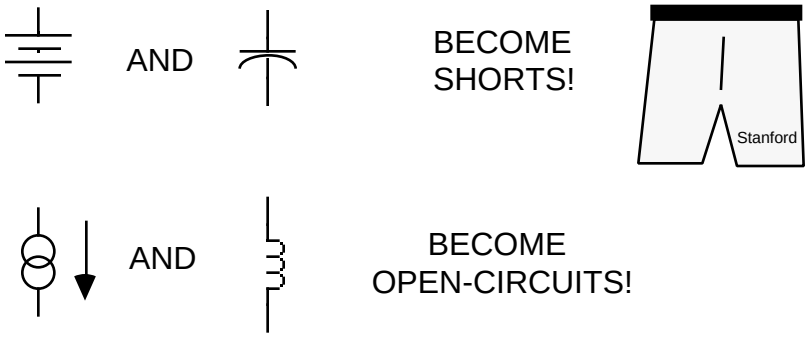
• The concept of g_m and r_π can be usefully combined to obtain the

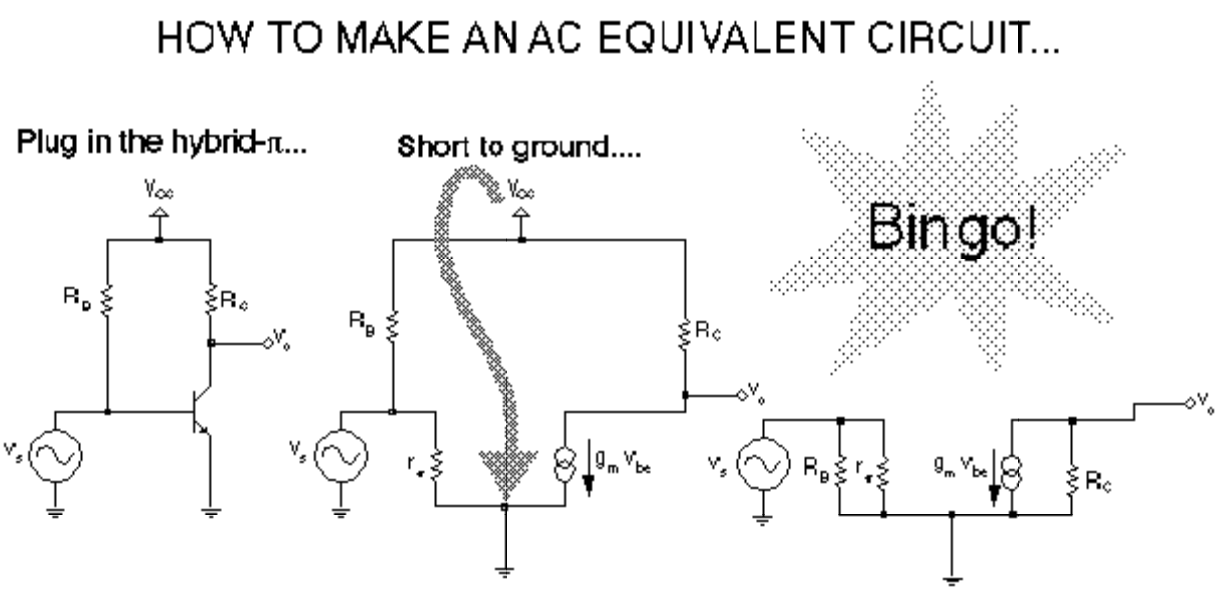
7: HYBRID-π MODEL FOR (AC) SMALL SIGNALS



• This simple model for the BJT can be plugged into amplifier circuits to figure out gain, etc. More detailed versions include parasitic capacitances and resistances.

• **REMEMBER that for AC analysis, the DC power supply voltages get shorted to ground, capacitors become short-circuits, and current sources (other than those defined as AC signals, as above) become open-circuits!**





NOTE that the small-signal equivalent circuit shown above works for NPN or PNP transistors with NO CHANGE OF POLARITY!!!

It is CRITICAL, however, to consider the differences between NPN and PNP transistors when analyzing the DC bias conditions!

It is important to keep in mind the effect that the DC bias conditions (particularly I_C) have on the AC model... basically, I_C directly controls g_m and hence the gain when used in an amplifier circuit!

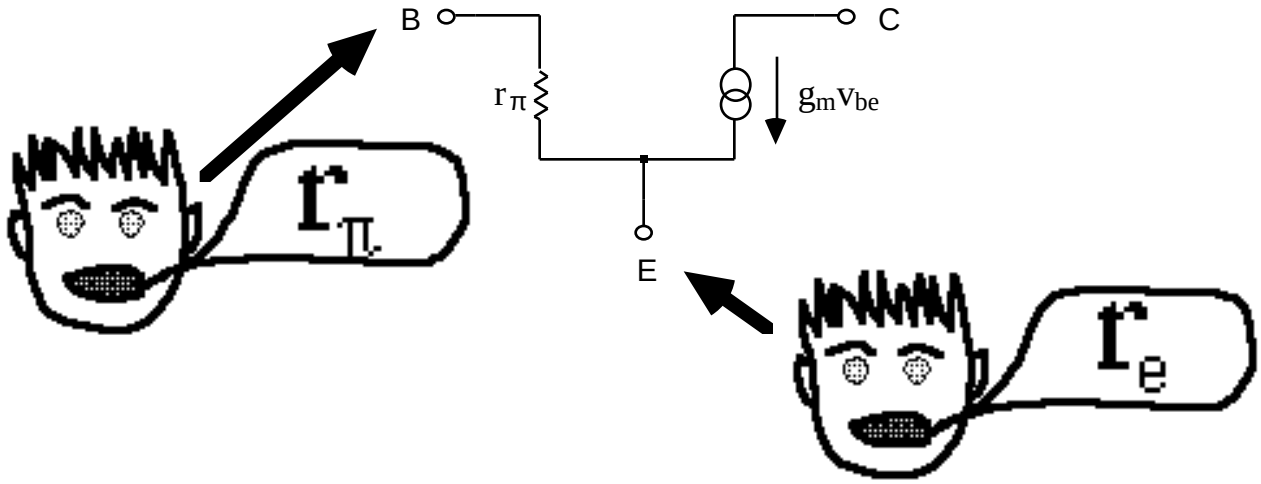
8: SCALING RESISTANCES BETWEEN BASE AND EMITTER

• The resistance between base and emitter depends on which way you look!

• The conceptual explanation is: from the base's viewpoint, a small change in voltage causes a relatively small change in base current, but from the emitter's viewpoint, a small change in voltage (a change in v_{be}) causes a much larger change in current due to the g_m generator!

•This means the emitter-to-base resistance, r_e seems much smaller... looking in through the emitter, a small change in the voltage relative to the base causes a huge amount of current to flow (compared to the same change in voltage applied looking into the base) because you get not only the base current flowing through r_π, but also the extra current from the transistor's amplifying action.

• Looking into the base toward the emitter, one "sees" r_π

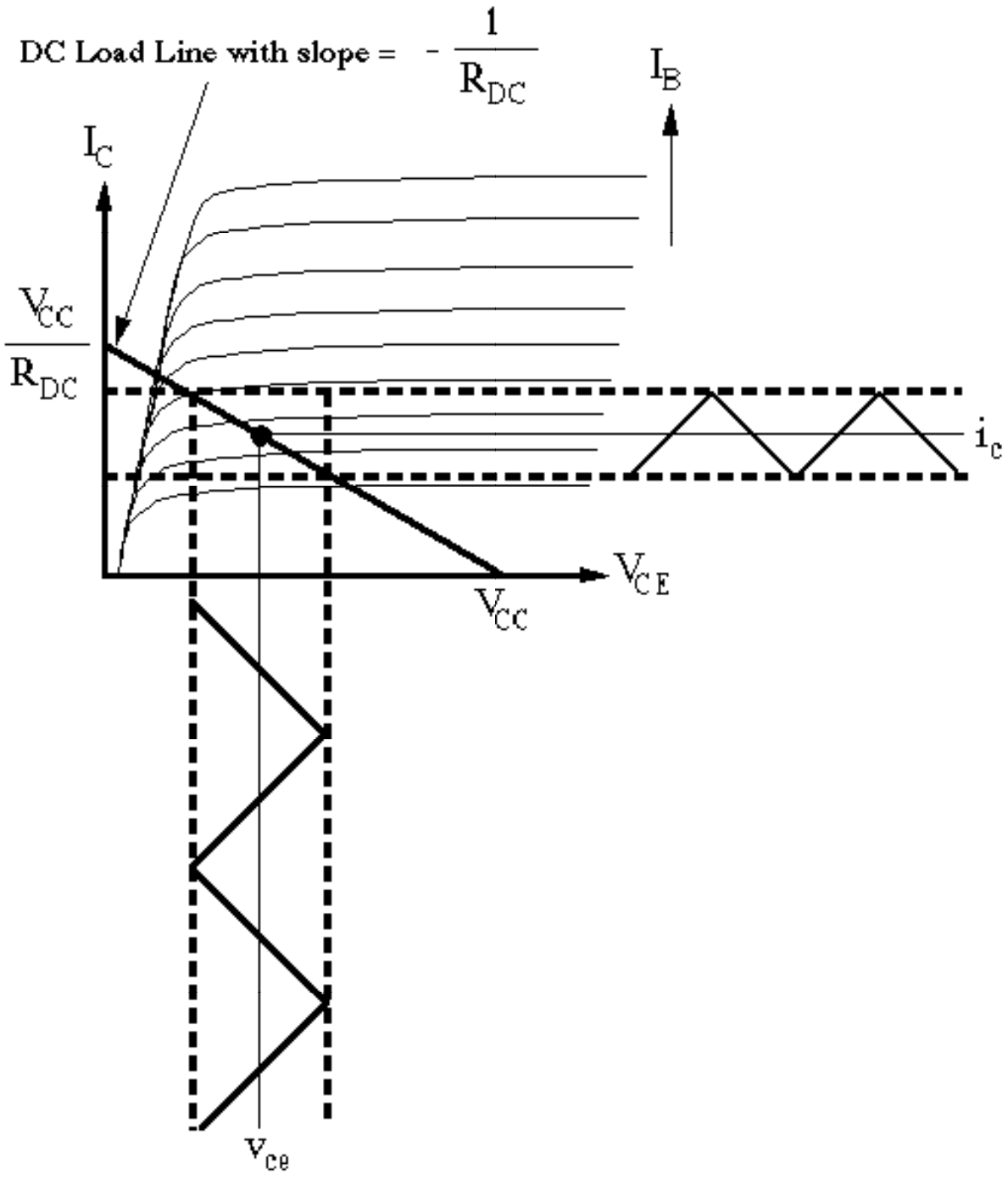


• Looking into the emitter toward the base, one "sees" r_e. For a change in emitter voltage, (β + 1) times as much current change will occur than for a comparable voltage change at the base. Therefore,

$$r_e = \frac{r_\pi}{(\beta + 1)} \qquad \text{also...} \quad r_e \approx \frac{r_\pi}{\beta} = \frac{1}{g_m}$$

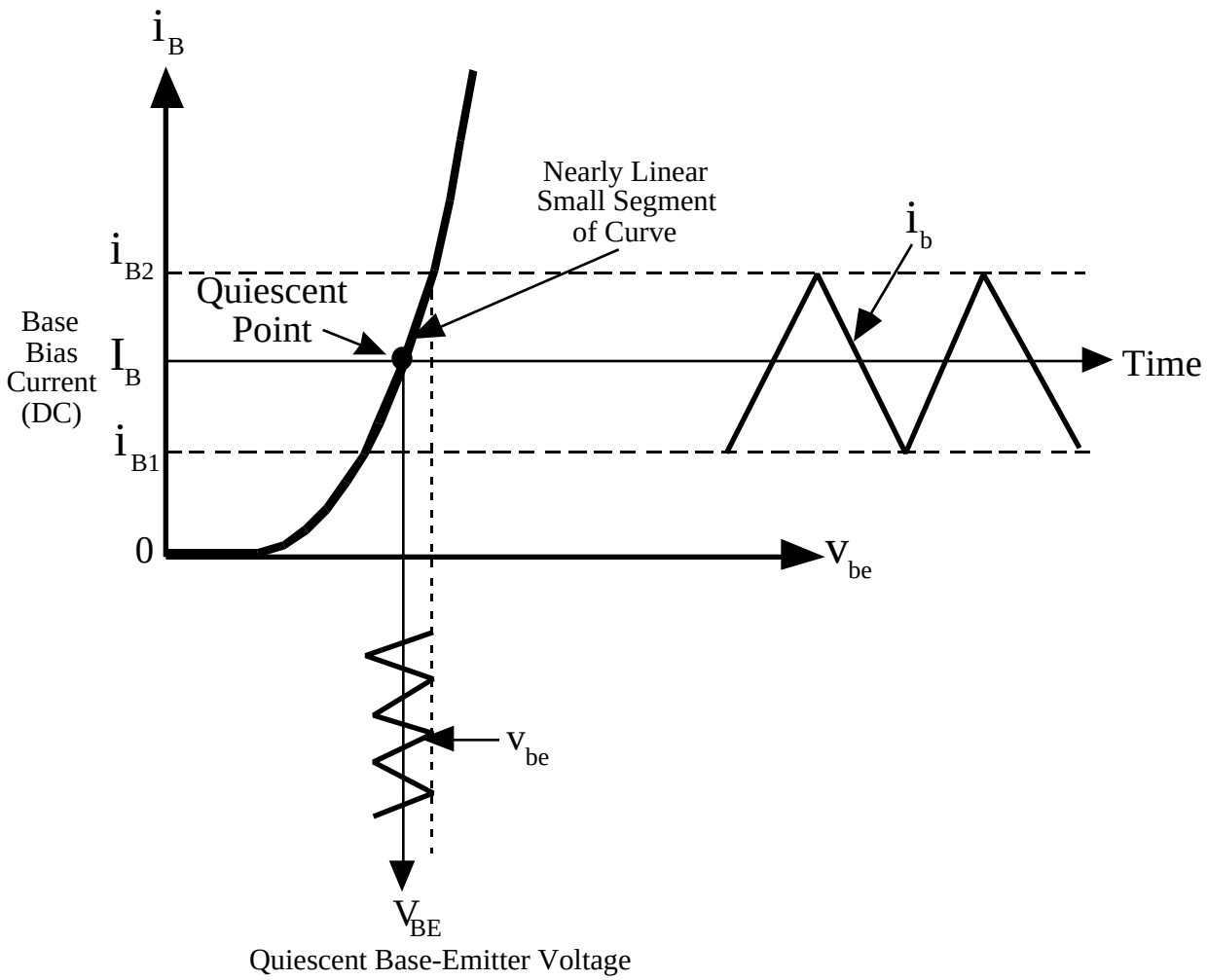
KEY POINT: You can "transform" a resistance from the emitter or base side of the base-emitter circuit to the opposite side by multiplying by (β + 1) if looking in the base, or dividing by (β + 1) if looking in the emitter.

9: AC LOAD LINES



• The idea here is to extend the DC load line concept to allow for “wiggling” the base current using an applied (AC) signal and looking at the corresponding “wiggling” of V_{CE} along the constraining line of the resistor (Ohm’s Law) to see what the output of the amplifier is doing (i.e. how much it is amplifying).

• The plot below shows how the base current, i_b, varies with v_{be}. Such variations in i_b lead to variations in collector current (and finally output voltage) by causing the movement between the various I_C vs V_{CE} curves shown above (movement from one line to the other on the plot is constrained by the output resistor load line, giving rise to the output voltage waveforms shown).



Chapter 4: Operational Amplifiers

Op-amps are great, op-amps are neat,
between you and me, they just can't be beat...
Former EE113 Brown-Nosing Student
Presently employed as freelance poet.

1: OBJECTIVES

• To learn:

what an op-amp is...

the basic op-amp circuits

the differences between "ideal" and "real" op-amps

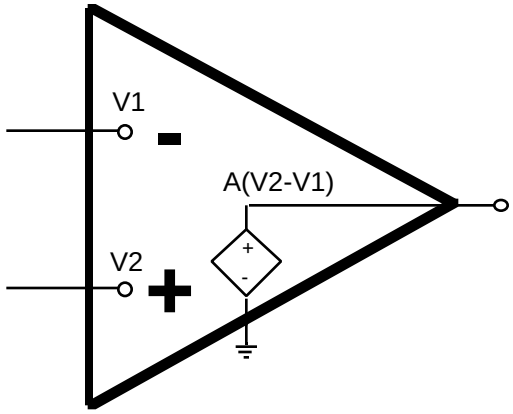
the frequency response of op-amps

a bit about feedback

READ S&S CHAPTER 2

2: OPERATIONAL AMPLIFIERS CONCEPTS

• Op-amps are amplifiers that provide the amplified difference between two input signals as their output...



1) **The input impedance is infinite** - i.e. no current ever flows into either input of the op-amp.

2) **The output impedance is zero** - i.e. the op-amp can drive any load impedance to any voltage.

3) **The open-loop gain (A) is infinite.**

4) **The bandwidth is infinite.**

5) **The output voltage is zero when the input voltage difference is zero.**

COMMENTS ON FEEDBACK (more later!)

• The gain of the circuit is made less sensitive to the values of individual components.

• Nonlinear distortion can be reduced.

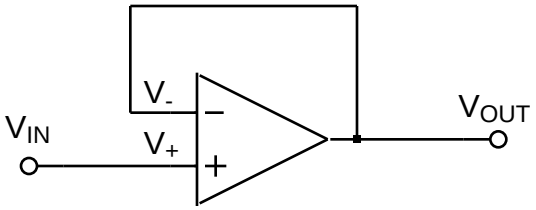
• The effects of noise can be reduced.

• The input and output impedances of the amplifier can be modified.

• The bandwidth of the amplifier can be extended.

3: BASIC OP-AMP CIRCUITS

3.1 VOLTAGE FOLLOWER



• Note that the op-amp can swing its output in either direction to keep the voltage difference between the input zero.

$V_- = V_{OUT}$

substitute into the basic op-amp equation to get...

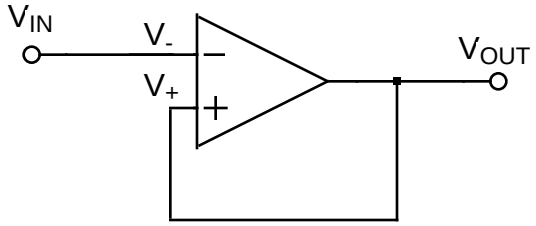
$V_{OUT} = A(V_+ - V_-)$ $\quad V_{OUT} = A(V_{IN} - V_{OUT})$ $\quad (1 + A)V_{OUT} = AV_{IN}$

which yields,

$$V_{OUT} = \frac{A}{(1 + A)}V_+ \qquad V_{OUT} = V_+ \qquad \text{as } A \to \infty$$

• Here the input impedance is that of the op-amp itself (very high).

• What about this configuration? Does it work?



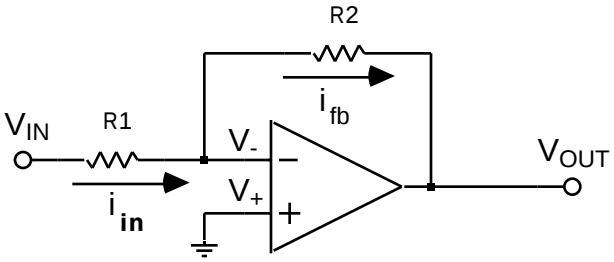
• Well, if you do the math, it looks like it should...

$$V_{OUT} = A(V_+ - V_-) = A(V_{OUT} - V_-)$$

$$V_{OUT} = \left(\frac{A}{1 - A}\right)V_- \;\rightarrow\; V_{OUT} = -V_- \text{ as } A \to \infty$$

• This would work only if the op-amp had no poles (response flat out to infinite frequency)... if you have any poles, they can move to the right half-plane and the whole thing oscillates (positive feedback).

3.2 INVERTING AMPLIFIER



• By definition, $v_{out} = A(v_+ - v_-)$ and thus, $v_+ - v_- = \frac{v_{out}}{A}$ which means that as A approaches infinity, $(v_+ - v_-) \rightarrow 0$ (this is the virtual ground assumption). Since, for an ideal op-amp, the input impedance is infinite, the input current is zero. This means that the current in through R_1 must come out via R_2 and none enters the v_- terminal. This means that one can write,

$$\frac{v_{in}}{R_1} + \frac{v_{out}}{R_2} = 0 \quad \text{which gives} \quad A_V = \frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1}$$

• Note that the input impedance is simply R_1 since it is connected to a virtual ground...

KEY POINT: With negative feedback (as is generally used with op-amps except as oscillators or comparators), the two input terminals are forced to the same potential by the feedback.

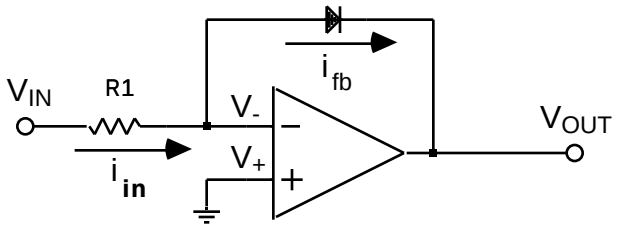
If v_+ is grounded, v_- is also forced to ground. This is a common configuration, and we refer to the v- terminal as a "virtual ground."

If v_+ is not grounded, v_- is still forced to the same voltage that is applied to v_+.

This simple rule makes op-amp analysis quite simple in many cases.

3.3 LOGARITHMIC AMPLIFIER

• Replace R_2 of the Inverting Amplifier with a diode....



• Start with the diode transfer function,

$$I_{diode} = I_s\left(e^{\frac{v}{nv_T}} - 1\right) \approx I_s e^{\frac{v}{nv_T}} \quad \text{thus, the feedback current is } i_{fb} \approx I_s e^{\frac{v_- - v_{out}}{nv_T}}$$

(assume n = 2 for discrete diodes)

• Using the virtual ground assumption,

$$i_{in} = \frac{v_{in}}{R_1} \quad \text{and} \quad i_{fb} \approx I_s e^{\frac{-v_{out}}{nv_T}} \quad \text{(remember that for an inverting amp, } i_{fb} = -\frac{v_{out}}{R_2}\text{)}$$

and their sum must be equal to zero since no current enters the v_- terminal.

• We also know that,

$$v_{out} = -nv_T \ln\left(\frac{i_{fb}}{I_S}\right) = -nv_T\left[\ln(i_{fb}) - \ln(I_S)\right]$$

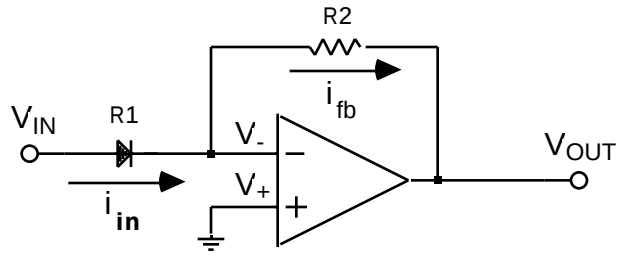
• Since $i_{fb} = i_{in}$, one can substitute $i_{in} = \frac{v_{in}}{R_1}$ for i_{fb}...

$$\boxed{v_{out} = -nv_T\left[\ln\left(\frac{v_{in}}{R_1}\right) - \ln(I_S)\right]}$$

• In practice, this circuit would probably not be used for a log amplifier. Instead, one would use a grounded-base transistor in place of the diode to eliminate the effect of the "n" term (dependent upon the current through the diode) and also take advantage of the fact that the exponential i-v relationship extends over a much larger range for transistors.

3.4 EXPONENTIAL AMPLIFIER

• Replace R_1 of the Inverting Amplifier with a diode.



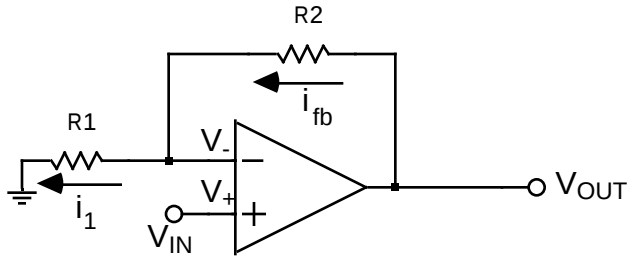
• Note that $i_{in} \approx I_s e^{\frac{v_{in}}{nv_T}} = -\frac{v_{out}}{R_2}$ and thus, $v_{out} = -R_2 I_s e^{\frac{v_{in}}{nv_T}}$

• With exponential and logarithmic functions, one can multiply and divide if one can add and subtract (this is easy with op-amps, as discussed below)! This is accomplished as follows:

$$A \times B = e^{[\ln(A)+\ln(B)]} \qquad \frac{A}{B} = e^{[\ln(A)-\ln(B)]}$$

• This principle, along with the addition, subtraction, integral and derivative op-amp functions described below, were the basis for analog computers.

3.5 NON-INVERTING AMPLIFIER



• Since feedback is operating, the op-amp tries to hold the difference between its input terminals at zero (remember the idea behind the virtual ground assumption... this is similar). Again, if you write the basic op-amp equation, and substitute v_{in} for v_+,

$$v_{out} = A(v_+ - v_-) = A(v_{in} - v_-) \quad \rightarrow \quad \frac{v_{out}}{A} = (v_{in} - v_-)$$

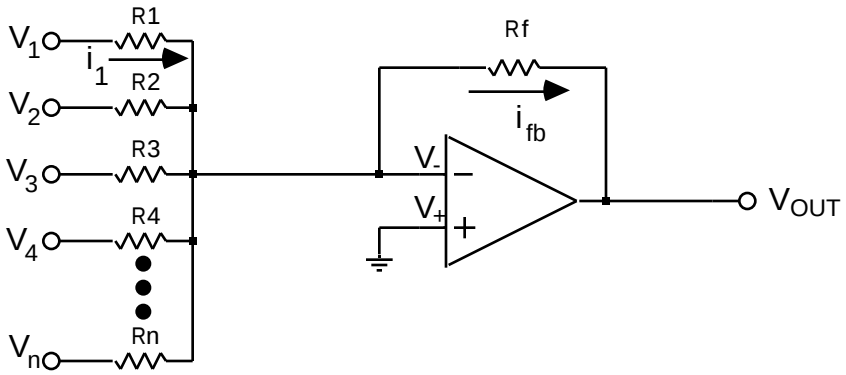
Thus, as the op-amp's gain A becomes very large, the difference between vin and v_- must go to zero. This means that $v_{in} = v_-$ if A goes to infinity. In other words, the voltage at the v_- terminal is forced to equal the input voltage.

• Thus, start with the assumption that, $v_- = v_+ = v_{in}$, and, considering the fact that no current will enter the op-amp terminals, write,

$\frac{v_{out} - v_{in}}{R_2} - \frac{v_{in}}{R_1} = 0$ which can be rearranged to yield, $\frac{v_{out}}{v_{in}} = \left(1 + \frac{R_2}{R_1}\right)$

• This circuit is very useful when you need to use the full input impedance of the op-amp, such as in instrumentation. (Of course, you can obtain a non-inverting amplifier by connecting two inverting amplifiers in series, but that uses on additional amplifier.)

3.6 SUMMING AMPLIFIER



• This amplifier's operation can be "summed up" by this equation, indicating that the input and feedback currents must add up to zero (no current enters the operational amplifier's input terminals), $\sum_{k=1}^{n} i_k + i_{fb} = 0$

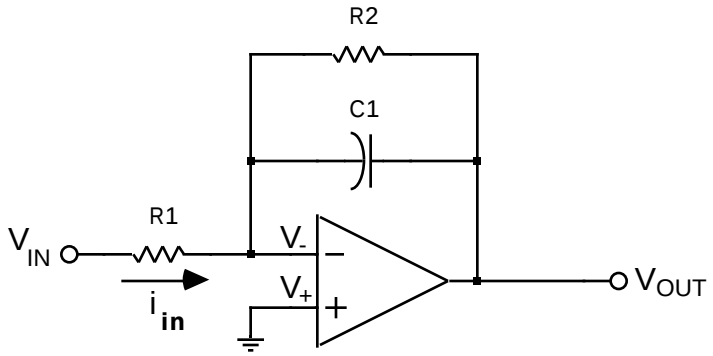
• Summing currents, one can write, $\frac{v_{out}}{R_f} = -\left(\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} + \cdots + \frac{v_n}{R_n}\right)$

Which can be rearranged to give, $v_{out} = -\left(v_1 \frac{R_f}{R_1} + v_2 \frac{R_f}{R_2} + v_3 \frac{R_f}{R_3} + \cdots + v_n \frac{R_f}{R_n}\right)$ which has the form of a series of "n" inverting amplifiers, whose outputs are summed together.

• The summing amplifier is often used as an audio mixer, where the inputs are voltages from several microphones or other sources, and the input resistors, R_1 ••• R_n are varied to control the individual channel gains.

• This circuit can also be used as an averager if $R_1 = R_2 =$ ••• $= R_n$ and $R_f = (R_1/n)$

3.7 INTEGRATOR



• For DC, it is just like an inverting amplifier,

$$\frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1}$$

• For higher frequencies, the capacitor begins to matter,

$$\frac{v_{in}}{R_1} = -C_1 \frac{dv_{out}}{dt}$$

• It is simplest to replace R_2 for the inverting amplifier with the impedance of the parallel combination of R_2 and C_1,

$$\frac{v_{out}}{v_{in}} = -\frac{Z_2}{R_1} = -\frac{\left(\frac{1}{C_1 S} \| R_2\right)}{R_1} = -\frac{\left(\frac{R_2}{C_1 S}\right)}{\left(R_2 + \frac{1}{C_1 S}\right)} = -\frac{\left(\frac{R_2}{R_2 C_1 S + 1}\right)}{R_1} = -\frac{R_2}{R_1 (R_2 C_1 S + 1)}$$

• The form of this equation is a low-pass filter with a cut-off frequency of $f_c = \frac{1}{2\pi R_2 C_1}$ (we will refer to it as f_{min}) and a DC gain of $\frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1}$

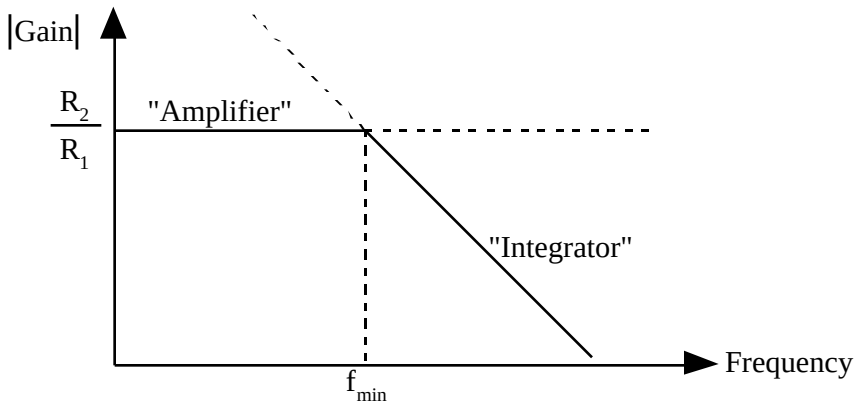
• This is, in fact, an integrator for frequencies above f_c, and an inverting amplifier for frequencies below f_c. (When you see capacitors in a circuit, always consider what happens at zero and infinite frequency!)

• For the theoretical “ideal” integrator circuit, R_2 would be omitted, and the equation would be,

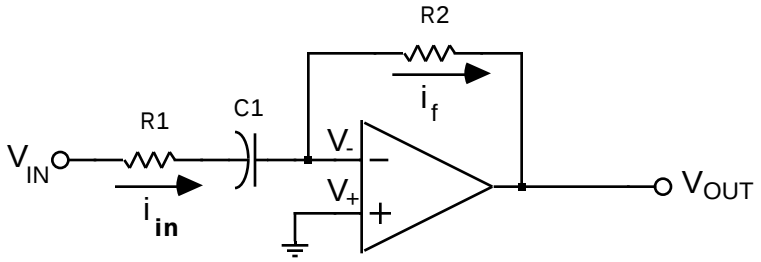
$$v_{out} = -\frac{1}{R_1 C_1}\int v_{in}\,dt$$

• However, small DC offsets at the input (and those of realistic, "non-ideal" op-amps) would quickly "charge up" the integrator... remember that the integral of a constant is the constant times time! We want to limit the integrator's theoretical infinite gain at DC to something less.

• For the realistic integrator shown above, the integral equation is correct, but only for frequencies above the point where the effect of C_2 begins to dominate over R_2 to set the gain of the circuit. The frequency below which the circuit’s behavior becomes more like a DC amplifier than an integrator is given by the low-pass filter's cut-off frequency.



3.8 DIFFERENTIATOR



• In the differentiator circuit shown here, there is also a component, R_1, that is sometimes not shown in “textbook” op-amp differentiator circuits.

• Its purpose is to limit the high-frequency gain of the differentiator so that it does not get swamped by high frequency noise (which may have a large derivative despite a small amplitude).

• For “low-enough” frequencies that the input impedance is dominated by C_1, i_{in} and i_f can be equated to show that,

$$v_{out} = -R_2 C_1 \frac{dv_{in}}{dt}$$

• As for the integrator above, there is a frequency range over which the differentiator will not work very well.

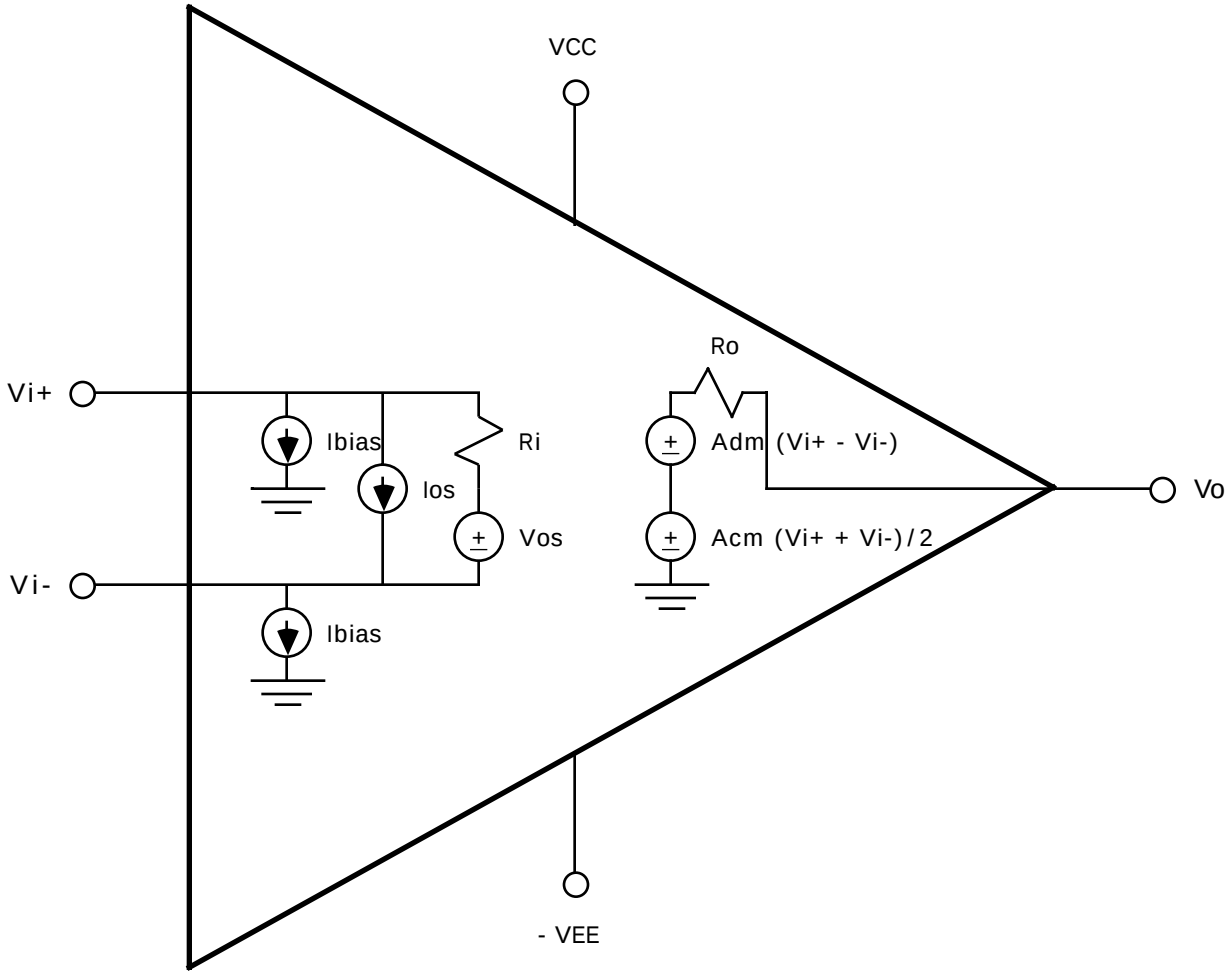
• Again, one can start with the equation for an inverting amplifier and substitute the impedance of R_1 and C_1 in series for R_1,

$$\frac{v_{out}}{v_{in}} = -\frac{R_2}{Z_1} = -\frac{R_2}{R_1 + \frac{1}{C_1 S}} = -\frac{R_2 C_1 S}{R_1 C_1 S + 1}$$

which yields an equation for a high-pass filter in classical form, with a cut-off frequency of, $f_{max} = \frac{1}{2\pi R_1 C_1}$, above which the filter gives a steady gain of $\frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1}$ and below which it acts as a differentiator.

• Again, substitute zero and infinity for S in the above equation and be sure you understand what happens at both limits.

4: “REAL” VERSUS “IDEAL” OP-AMPS



• There are unwanted currents at the inputs!

• There are offset currents and voltages!

• Signals applied to both inputs (which should not be amplified) are amplified to some extent!

• The input resistance is not infinity!

• The output resistance is not zero!

• However, for most practical applications, they are pretty close to being ideal, and negative feedback helps make them even closer!

5: FREQUENCY RESPONSE OF OP-AMPS

• As you might have guessed, op-amps do ***not*** have infinite frequency response either...

• When used without external feedback, the op-amp is in **OPEN-LOOP** mode, and the gain is quite large, but the frequency response is **TERRIBLE**!.

• As you increase the amount of negative feedback, the bandwidth increases and the gain decreases.

• The product of **GAIN X BANDWIDTH** is a constant for a given op-amp (guess what?... it is referred to as the “gain-bandwidth product”).

• The op-amp has (by design) a **FIRST-ORDER LOW-PASS RESPONSE**, as we saw in the first lectures....

• The open-loop gain is given by:

$$A_{op-amp}(S) = \frac{A_o}{1 + \frac{S}{\omega_o}}$$

where A_o is the open loop gain at DC and ω_o is the 3-dB or “break” frequency at which the *open-loop* gain starts to roll off.

KEY POINT: You can model an op-amp’s open-loop frequency response as a first-order RC low-pass filter with,

$$\omega_o = \frac{1}{(RC)_{equivalent}}$$

• Another key definition is the **UNITY-GAIN BANDWIDTH**, which is the frequency, ω_t, at which the gain reaches **ONE**.

• By thinking about the gain-bandwidth product concept, it follows that,

$$\omega_t = A_o \omega_o$$

• If you re-derive the gain equation for the inverting amplifier assuming a finite op-amp gain (see page 55, Sedra & Smith), you obtain,

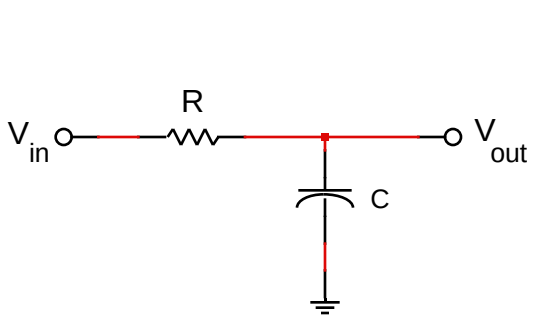
$$A_v(S) = -\frac{\frac{R_2}{R_1}}{1+\frac{\left(1+\frac{R_2}{R_1}\right)}{A_{op-amp}(S)}}$$

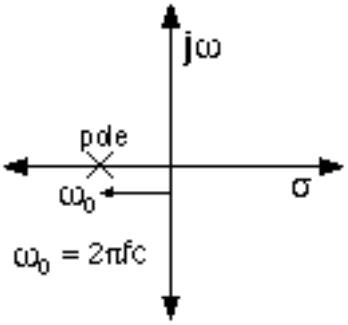
• Substituting the op-amp's frequency response in for $A_{op\text{-}amp}$, you (eventually) obtain,

$$A_v(S) = -\frac{\frac{R_2}{R_1}}{1+\frac{\left(1+\frac{R_2}{R_1}\right)}{\frac{A_o}{1+S\omega_o}}} = -\frac{\frac{R_2}{R_1}}{1+\frac{1}{A_o}\left(1+\frac{R_2}{R_1}\right)+\frac{S}{\frac{\omega_t}{1+\frac{R_2}{R_1}}}}$$

$$A_v(S) \approx -\frac{\frac{R_2}{R_1}}{1+\frac{S}{\omega_t}\left(1+\frac{R_2}{R_1}\right)} \quad \text{for} \quad A_o >> \left(1+\frac{R_2}{R_1}\right)$$

• This is a first-order low-pass filter.





$$H(s) = \frac{K}{1 + \frac{s}{\omega_o}}$$ where K is the gain for low frequencies

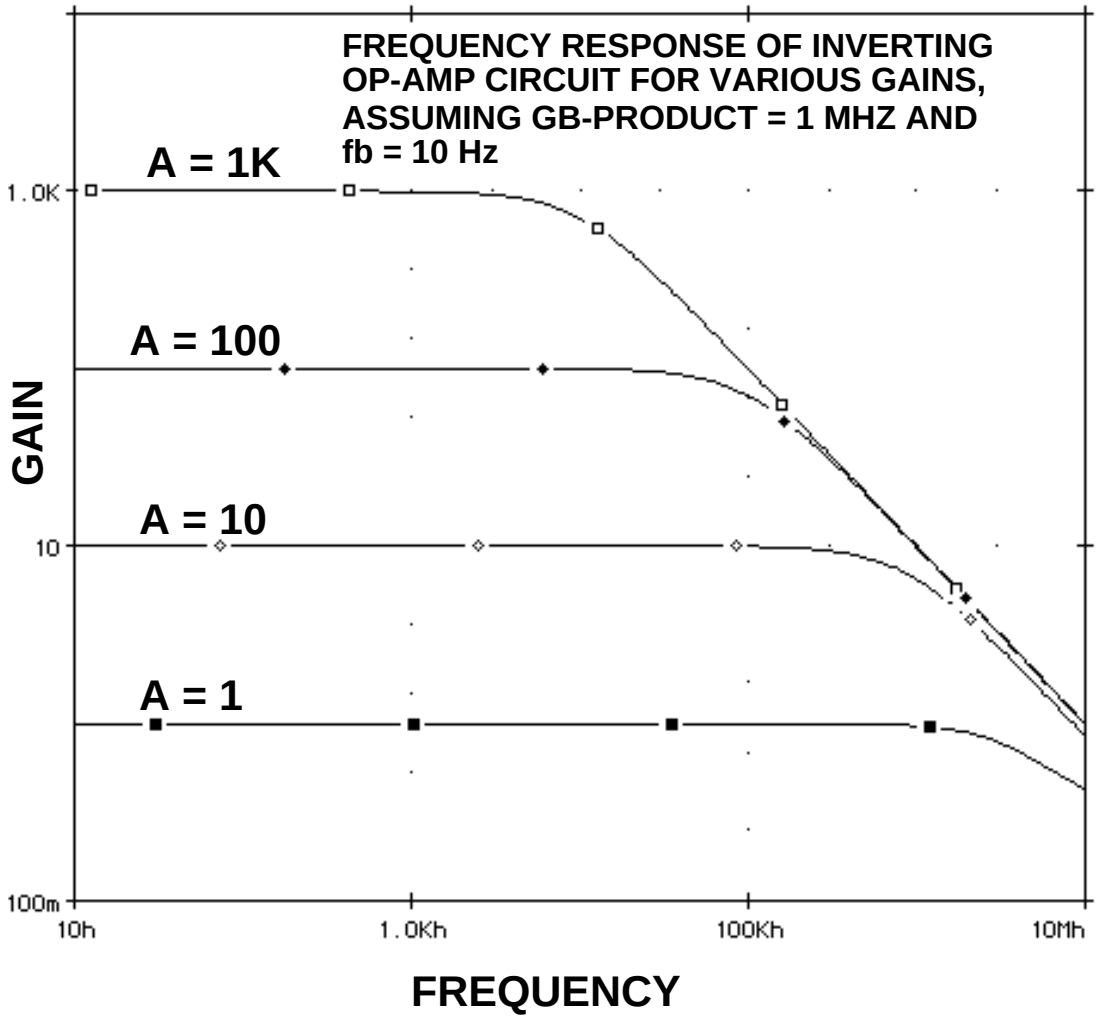
the pole is at $S = -\omega_o$ and the "cutoff" frequency is at $\omega_0 = 2\pi f_c = \frac{1}{RC}$

THE DC GAIN IS $-\frac{R_2}{R_1}$ **AND THE BREAK FREQUENCY IS** $\frac{\omega_t}{\left(1 + \frac{R_2}{R_1}\right)}$

CONCLUSION: You can model the frequency response of the inverting configuration also using a first-order low-pass filter with,

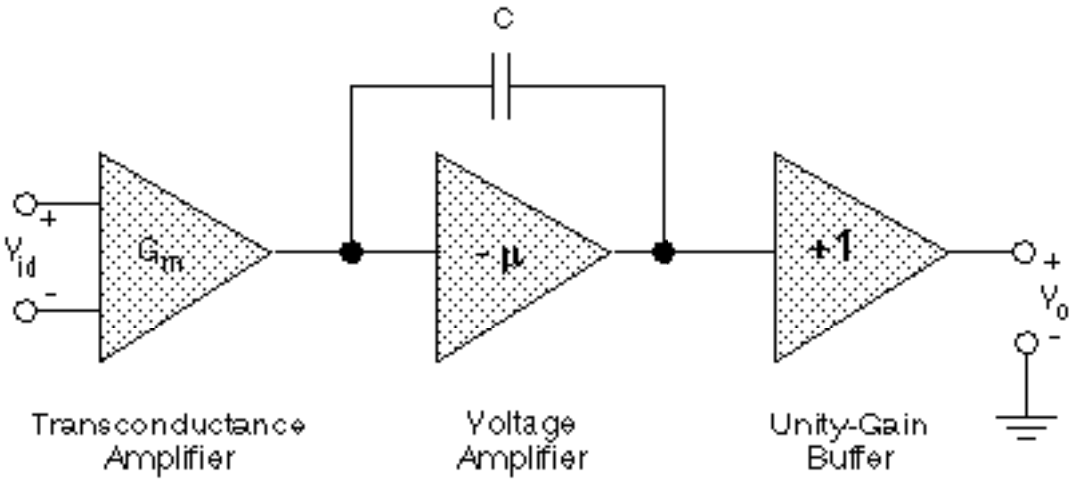
$$RC_{equivalent} = \frac{\left(1 + \frac{R_2}{R_1}\right)}{\omega_t}$$

• A similar analysis for the non-inverting case can be found in Sedra and Smith (Section 2.7).



• The above plots illustrate that, no matter what the gain of the op-amp is set to via external feedback resistors, the overall frequency response is constrained by the outer boundary set by the op-amp's open loop-roll off. As the gain is reduced, the frequency at which that new gain is reduced by 3dB moves up in frequency. This is another way of looking at the gain-bandwidth product rule.

6: THE GUTS OF REAL OP-AMP CHIPS



• In real op-amps, there is generally an internal (sometimes external) capacitor that sets the op-amp's ***dominant pole*** and forces it to roll off before other, less well controlled parasitic capacitances would cause that.

• In practical integrated circuit implementations, the capacitances available are very small (a few pF)... how can such small capacitances give rise to such low cut-off frequencies (a few hundred Hz)?

• The answer is provided by an understanding of the ***Miller Effect***, which basically explains how an impedance sitting across an amplifier is effectively converted into a smaller impedance at the input and roughly an equal impedance at the output of the amplifier... the amount that the effective input impedance is smaller than the actual one across the amplifier is a function of the amplifier's gain.

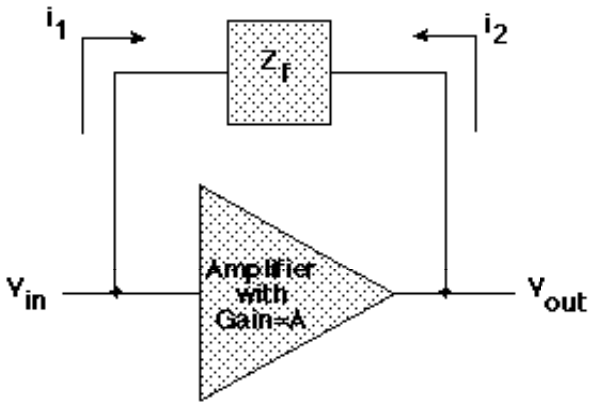
• This explains how an op-amp, with a huge gain and a very small internal capacitance, can act like it has a huge capacitance at its input (a smaller impedance corresponds to a larger capacitance).

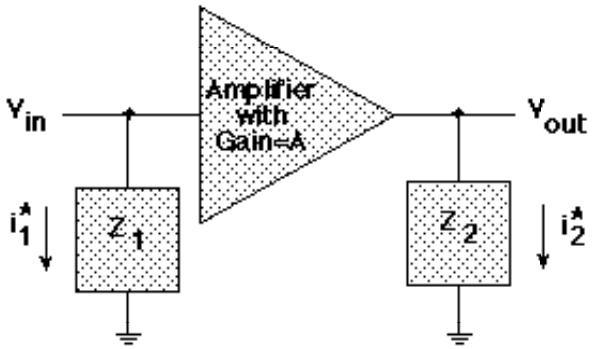
• As mentioned above, the Miller Effect effectively takes an impedance across an amplifier and replaces it with a smaller impedance at the input and a roughly equivalent one at the output.

• This effect works only for amplifiers that share a common terminal between input and output (e.g. ground).

• The effect does work for negative and positive gains, but for positive gains greater than one, gives rise to negative impedances at the input (reverse polarity of current that flows for an applied voltage, but Ohm's Law still applies). (The output impedance is still positive.)

• **Here, we only consider negative (inverting) amplifiers.**





$$i_1 = \frac{v_{in} - v_{out}}{Z_f} = \frac{v_{in} - Av_{in}}{Z_f} = \frac{v_{in}}{\frac{Z_f}{(1 - A)}}$$

$$i_2 = \frac{v_{out} - v_{in}}{Z_f} = \frac{v_{out} - \frac{v_{out}}{A}}{Z_f} = \frac{v_{out}}{Z_f\left(\frac{-A}{1 - A}\right)}$$

$$i_1^* = \frac{v_{in}}{Z_1} \qquad i_2^* = \frac{v_{out}}{Z_2}$$

By definition, $i_1^* = i_1$ **and** $i_2^* = i_2$

$$Z_1 = \frac{Z_f}{1 - A} \qquad Z_2 = Z_f \frac{-A}{1 - A}$$

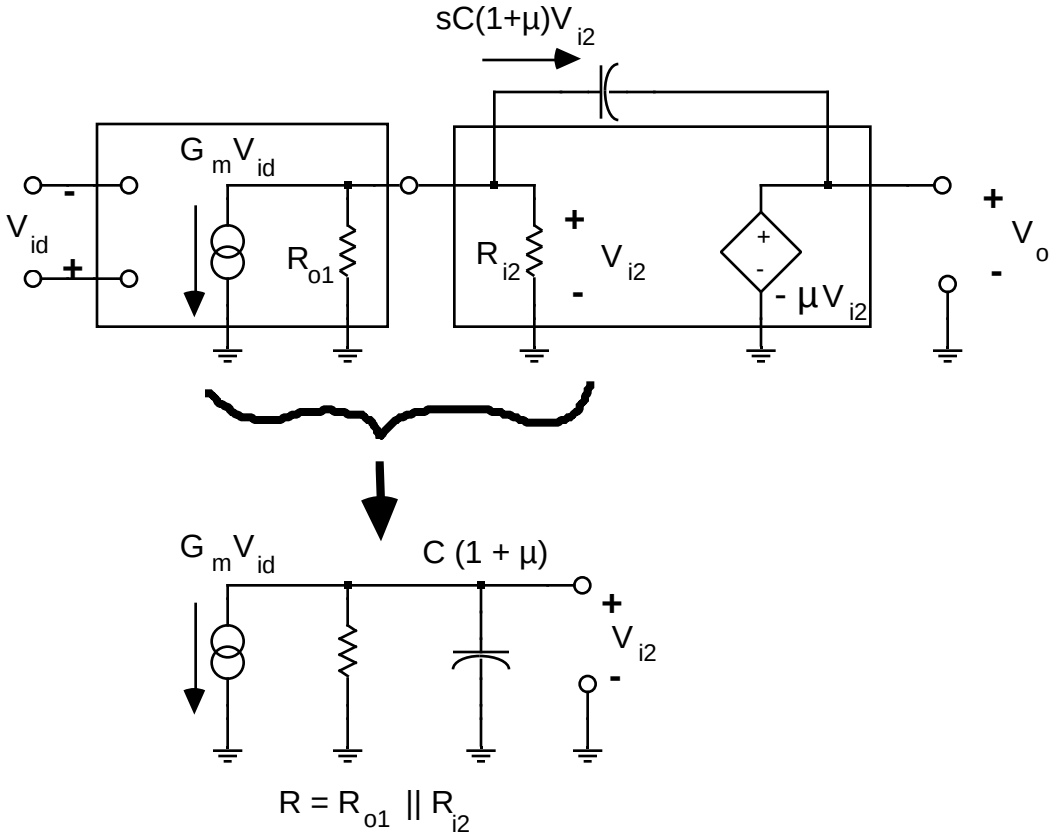
• Intuitively, one can think of “looking” into the input of the amplifier and seeing one side of an impedance... with an inverting gain, the amplifier is going to “pull” against the other side of that impedance in response to any input voltage wiggle...

• If you wiggle the input voltage up slightly and try to force current into the impedance (remember that you can’t force current into the input of the amplifier!), the amplifier will pull a lot more current away from you than if you were pushing against just the impedance tied to ground.

• This seems, “looking” from the input terminal, like a smaller impedance than what is sitting across the amplifier... you get more current flowing for a small voltage wiggle than if the impedance were just tied to ground.

• Note that taking A through the gain range of -1 to -∞, the corresponding range of Z_2 is $Z_2/2$ and Z_2. Thus for a capacitor in the Miller configuration, the maximum value of the effective C_{out} is $2C_f$ and the minimum is $C_{out} = C_f$.

• Using Miller’s Theorem, we can look at the op-amp “guts” model to figure out why we get the frequency response observed (after Sedra & Smith, Section 2.8)....

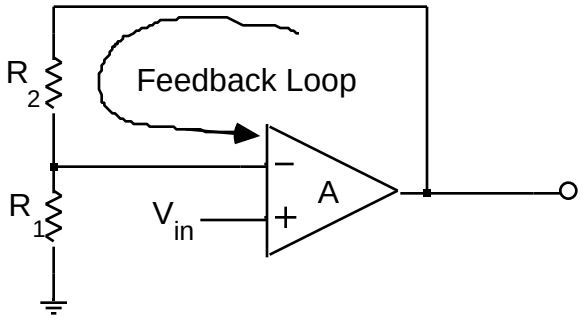


• From this it can be seen that the feedback capacitor’s value is multiplied by a factor of 1 + the gain of the internal voltage amplifier (μ) and placed in parallel with the combination of the first stage’s output resistance and the second stage’s input resistance.

• This determines the effective RC time constant of the op-amp (see the Appendix below).

• At the output, an equivalent capacitance is present with a value of C, for large µ... for an ideal (voltage source) output, that makes no difference, but for a real voltage source output (i.e. with a series resistance other than zero), it can make quite an important difference!

7: A PREVIEW OF FEEDBACK



• This schematic shows the feedback path for the non-inverting op-amp configuration.

• This is a useful point to define some of the feedback terms that will be used later in the course.

FEEDBACK RATIO (FACTOR) $\beta = \dfrac{R_1}{R_1 + R_2}$ ← In this case, it is just voltage division and ß is the fraction of the output voltage fed back.

LOOP GAIN: $T = -A\beta$

AMOUNT OF FEEDBACK $\equiv 1 - T = 1 + A\,\beta$

$$\text{GAIN} = \frac{A}{\text{AMOUNT OF FEEDBACK}} = \frac{A}{1 + A\beta}$$

$$\text{Gain} = A_V = \frac{A_o}{1 + A_o\left(\dfrac{R_1}{R_1 + R_2}\right)}$$

APPENDIX TO CHAPTER 4: A Bit More On Miller

Why isn't it called the Budweiser Effect?
Bobby Twistoffski
Stanford Senior, Electrical Engineering

WHY DO WE CARE?

• The Miller Effect can turn a small, parasitic capacitance sitting across an amplifier into a real problem!

• The Miller Effect is basically a multiplication of the capacitance's value, as seen at the input of the circuit by a factor related to the gain of the amplifier.

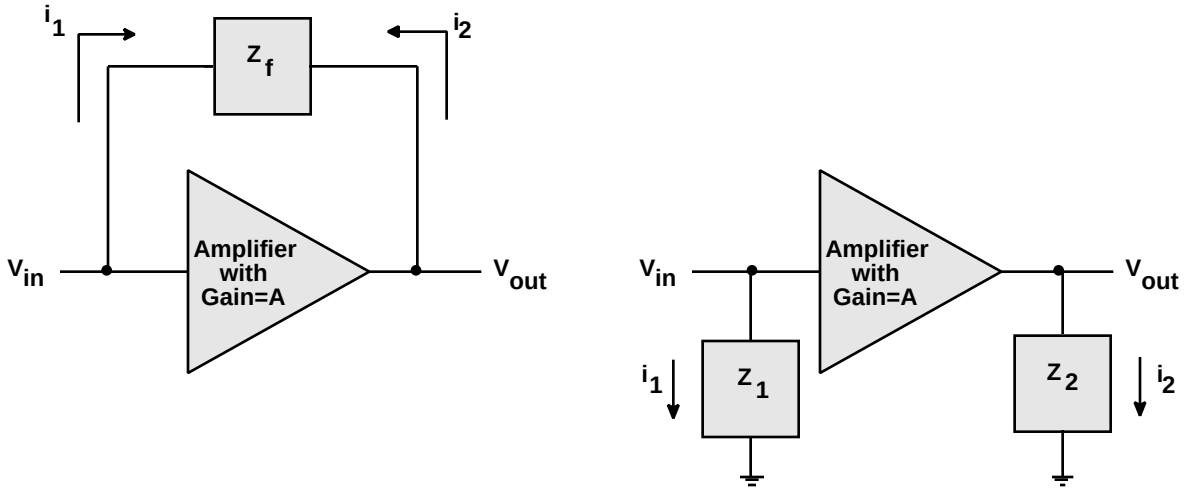
• In other words, we can get a HUGE effective capacitance at the input of a high-gain amplifier for having only a small (i.e. a few picoFarads) capacitance across it (from input to output)...

• We can use the Miller Theorem to help analyze circuits where we have an impedance across an amplifier.

• Again, that assumes that the gain of the amplifier is not changed by having the capacitor placed across it (if it is changed slightly, we can still use the Miller approximation).

• Previously, we saw that the Miller Theorem lets us "convert a circuit with an impedance across an amplifier in to one that is easier to analyze because we simplify it into two "separate" circuits!

• A **KEY** assumption is that the ***gain of the amplifier itself is not changed by having the impedance placed between its input and output...***



• We showed that,

$$Z_1 = \frac{Z_f}{1 - A} \qquad Z_2 = Z_f \frac{-A}{1 - A}$$

and for an "ideal" amplifier, we can let A -> ∞ and we get,

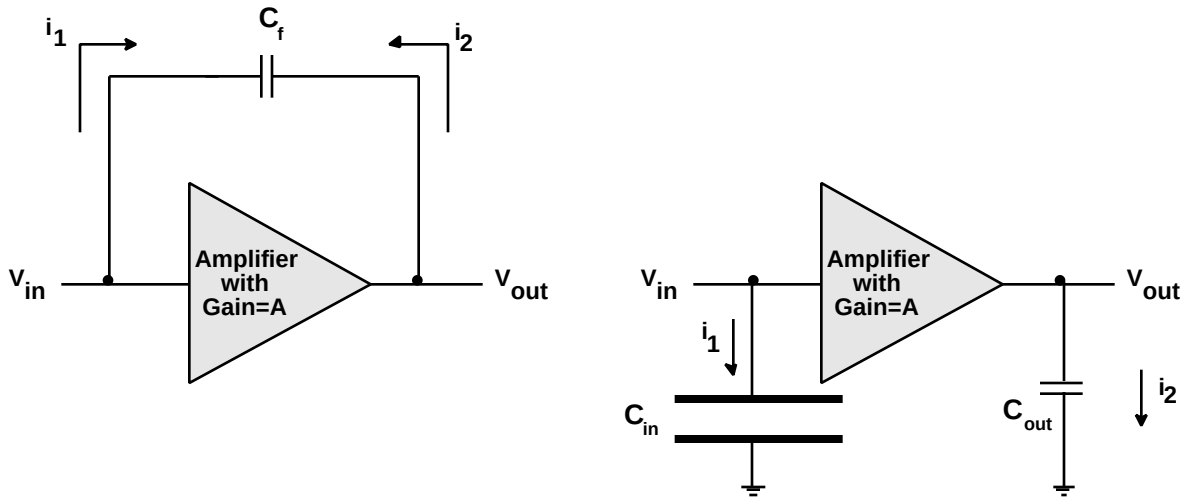
$$Z_1 \rightarrow 0 \qquad Z_2 \rightarrow Z_f$$

• We can replace an impedance across the amplifier to two impedances to ground (usually easier to work with).

• If our impedance was actually a capacitance, for a given frequency, that would mean that C_1 would tend to increase (to decrease the impedance at the input to zero) and C_2 would tend to decrease (to increase the impedance at the output to infinity).

• It's easier to call them C_{in} and C_{out} to keep things straight, and that is what we'll do...

• Now actually **do it** with a capacitor to convince yourself...



• The effective impedances are,

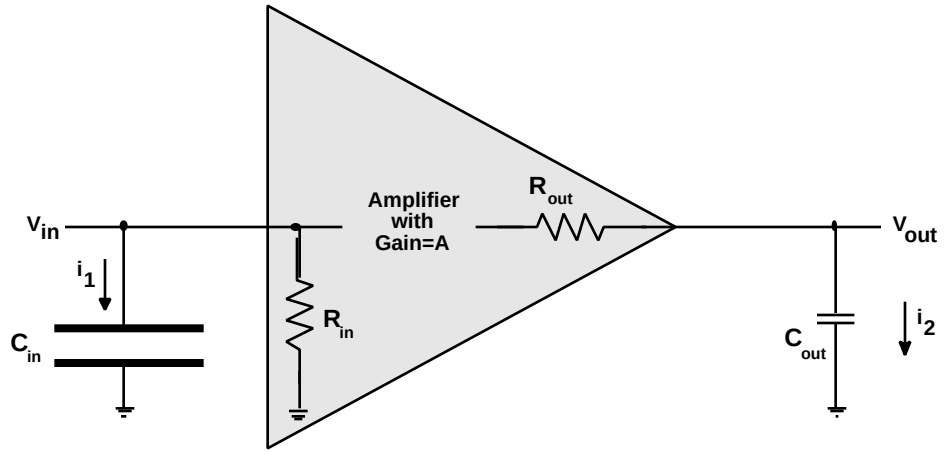
$$Z_{Cin} = \frac{\frac{1}{C_f S}}{1-A} = \frac{1}{C_f (1-A) S} \qquad Z_{Cout} = \frac{\frac{1}{C_f S}\left(\frac{-A}{1-A}\right)}{1} = \frac{1}{C_f \left(\frac{1-A}{-A}\right) S}$$

which is the same as saying that there are "scaled copies" of C_f at the input and output of the amplifier,

$$C_{in} = C_f (1-A) \qquad C_{out} = C_f \left(\frac{1-A}{-A}\right)$$

• If the amplifier was really "ideal" and we were not worrying about input and output resistances of the driving circuit and the load, these capacitances might not be a problem... (for example, if an "ideal" voltage source with zero output impedance was driving C_{in}, the fact that C_{in} was large would not matter)

• Now look at a "realistic" amplifier (input impedance is less than infinity and output resistance is greater than zero)...



• Now we have created two RC time constants (e.g. two low-pass filters!), one of which (input) turns out to usually be dominant in terms of the overall frequency response...

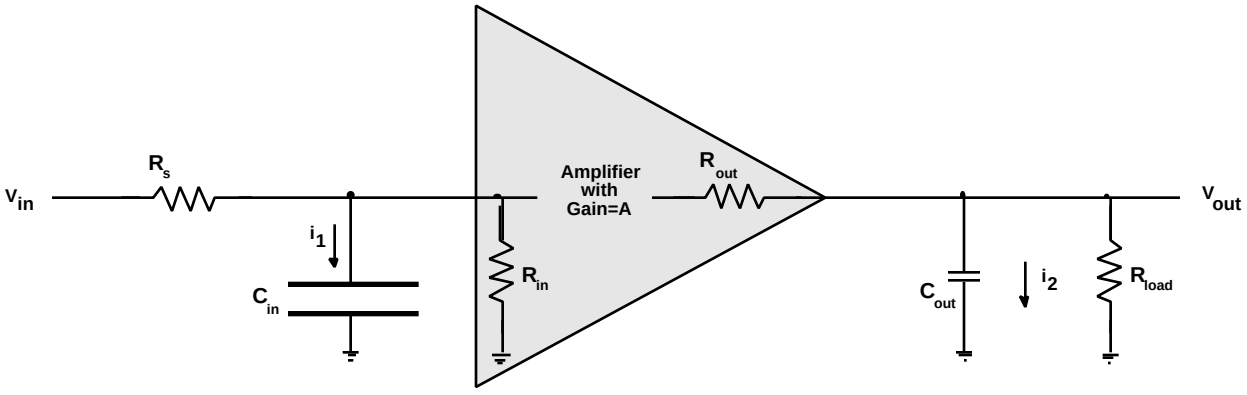
$$\tau_{in} = R_{in}C_{in} = R_{in}C_f(1-A) \qquad \tau_{out} = R_{out}C_{out} = R_{out}C_f\left(\frac{1-A}{-A}\right)$$

• From this you can see that we have a relatively small contribution from C_f at the output and a relatively large contribution at the input...

• For typical amplifiers, R_{in} is large and R_{out} is small, so we get a **large time constant at the input** and a small one at the output.

• In other words, the **input pole will dominate the frequency response** since it will take effect at a lower frequency that the output pole.

• Still more realistically, we have to take into account the output resistance of the circuit driving our amplifier and the load resistance that it has to drive... now we could compute more accurate time constants (and thus the frequency response).



Chapter 5: SINGLE-STAGE BJT AMPLIFIERS AND THE COMMON EMITTER AMPLIFIER

This amplifier goes to eleven!
Nigel, member of the rock band "Spinal Tap."

1: OBJECTIVES

• To learn about:

The similarities and differences between the three basic BJT amplifiers.

The basic analysis and design approaches to the common-emitter amplifier.

READ S&S Sections 4.10 - 4.12

2: OVERVIEW OF SINGLE-STAGE BJT AMPLIFIERS

• There are three basic BJT amplifier configurations, named depending upon which of the three terminals (B, C, or E) is **common** to the input and output of the amplifier (common-base, common-collector, or common-emitter, respectively).

• In practice, it is the terminal that is connected (either directly or through a capacitor bypassed resistor -> directly for AC signals) to a power or ground voltage that is the "common" terminal.

• Each of the three possible configurations has unique characteristics that make them useful in different situations. The table below compares the three basic configurations, as well as a variant of the common emitter amplifier.

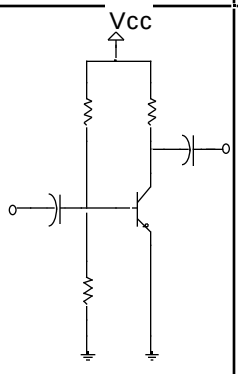
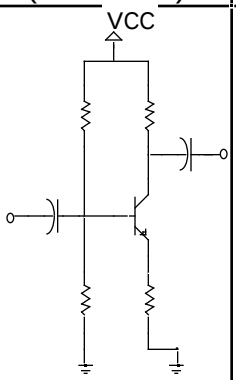
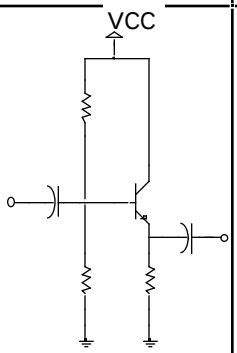
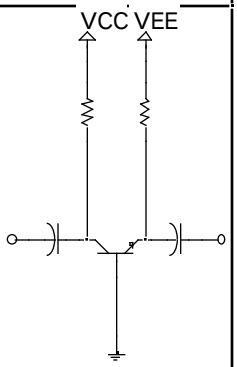
• The common emitter amplifier is the most common version, and is an *inverting* amplifier (that is, the output is 180° out of phase with the input). In many cases, a resistor is placed between the emitter and ground (usually bypassed with a large capacitor). This emitter resistor, R_E, serves to stabilize the bias point of the transistor using local feedback

(this is discussed in detail below). In order to obtain this stabilization, gain is traded off (reduced). This form of amplifier is, however, still a common emitter type.

• The common collector amplifier is often used as a buffer amplifier, since its *non-inverting* gain is almost exactly one. The current gain, however, is large (approximately ß+1), and this circuit is often used to add power to a signal.

• The common base amplifier, like the common collector, is *non-inverting*. It can provide high voltage gains, like the common emitter amplifier. The main difference between the common base and the other amplifier types is that the input impedance is very low. This can be a problem if the signal source is high impedance (in other words if the signal source cannot easily drive a low-impedance load), but it can be very useful if the signal source is low impedance (e.g. radio frequency signals arriving via a coaxial cable of characteristic impedance 50 Ω). The common base amplifier is generally very fast.

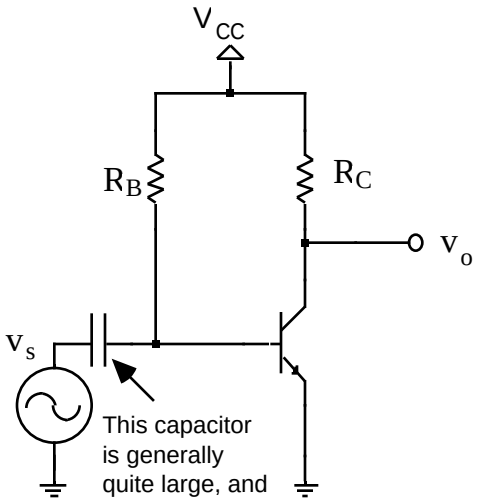
• The relative merits of each amplifier type is discussed below, including frequency response.

Parameter	**CE**	**CE with RE**	**CC**	**CB**
Inverting?	YES	YES	NO	NO
A_v	HIGH	HIGH (reduced)	LOW	HIGH
A_i	HIGH	HIGH (reduced)	HIGH	LOW
R_{in}	MEDIUM	MEDIUM (increased)	HIGH	LOW
R_{out}	HIGH	HIGH (increased)	LOW	HIGH
Typical Schematic				

3: THE COMMON EMITTER AMPLIFIER

• As mentioned above, the common emitter amplifier is by far the most common single-transistor amplifier configuration. You need to be quite familiar with it, its properties and, eventually, its variations. It is important to note that it is an **inverting** amplifier.

USING THE PREVIOUS EXAMPLE (not the best biasing, but simple)



$V_{CC} = 15V \qquad R_B = 50K$

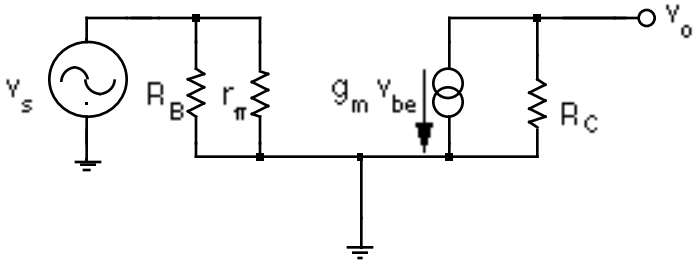
$R_C = 500\,\Omega \qquad \beta = 100$

$$I_B = \frac{15 - 0.7}{50K} = 0.286mA$$

$$I_C = 100\ I_B = 28.6mA$$

$v_o = -g_m v_{be} R_C$

$v_{be} = v_s$

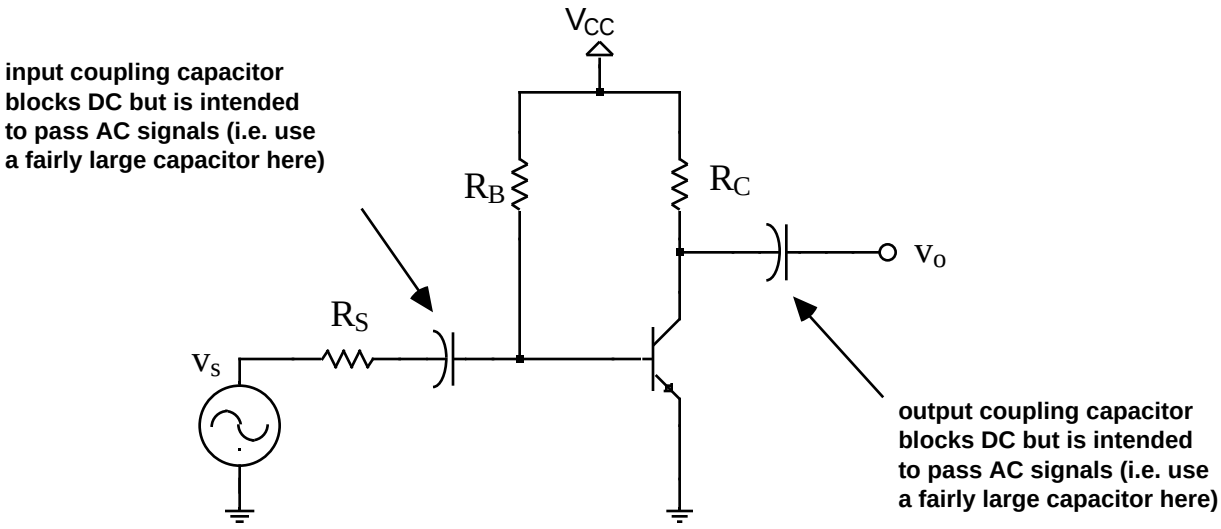


• One can compute the voltage gain A_v...

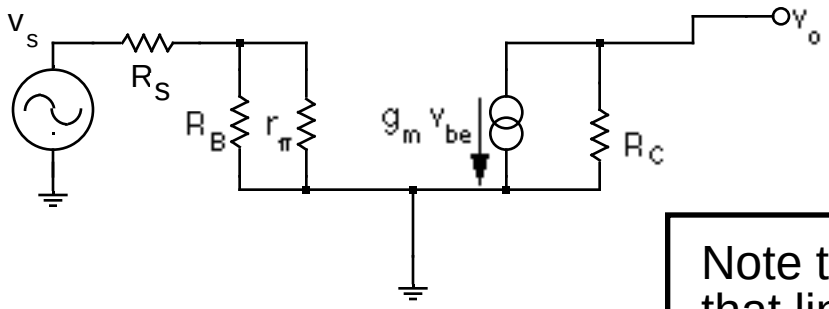
$$A_v = \frac{v_o}{v_s} = \frac{v_o}{v_{be}} = -g_m R_C$$

$$g_m = \frac{I_C}{V_T} = \frac{28.6\ mA}{25.9\ mV} = 1.1\,\Omega^{-1} \qquad A_v = -\,(1.1)(500) = -550$$

NOW MAKE IT MORE REALISTIC... ADD AN OUTPUT COUPLING CAPACITOR AND A SOURCE RESISTANCE!



• To make an AC small-signal model, short the caps and V_{CC} to ground and you get....



Note that it is I_c that links the DC and AC models through g_m

$$v_{be} = v_s \left(\frac{R_B \| r_\pi}{R_S + R_B \| r_\pi} \right)$$

$$v_o = -g_m v_{be} R_C$$

$$A_v = \frac{v_o}{v_s} = -\left(\frac{R_B \| r_\pi}{R_S + R_B \| r_\pi} \right) g_m R_C$$

• **Note** that with a source resistance, R_S, there is a voltage divider at the input, **reducing the gain.** The larger the source resistance is, the lower the gain will be. If the input resistance of the amplifier ($R_B \| r_\pi$ in this case) is made very large, the effects of R_S are reduced.

TRY THE EXAMPLE AGAIN WITH A 50 Ω SOURCE RESISTANCE (typical for a laboratory signal generator):

$R_B = 50\ K\Omega$ $R_C = 500\ \Omega$ $I_C = 28.6\ mA$ $\beta_F = 100$

$$g_m = \frac{I_C}{V_T} = \frac{28.6\ mA}{25.9\ mV} = 1.1\,\Omega^{-1} \qquad r_\pi = \frac{\beta}{g_m} = \frac{100}{1.1} = 90.6\,\Omega$$

$$A_v = -\ (1.1)(500)\left[\frac{50K \parallel 90.6\,\Omega}{50\Omega\ +\ 50K \parallel 90.6\ \Omega}\right]$$

$$\approx -\ (1.1)(500)\left[\frac{90.6}{50\ +\ 90.6}\right]$$

$$= -356 \quad \text{Not Bad!}$$

• REMEMBER this is **SMALL** signal only! (i.e. $v_{be} << v_T = 25.9$ mV) Note that $V_C \approx 0.7$ V, and the transistor is on the edge of saturation. Running it at a lower current would raise V_C and allow for a larger voltage swing at the output, but would reduce gain.

• Things can get **nonlinear** for larger signals (i.e. **DISTORTION**)!

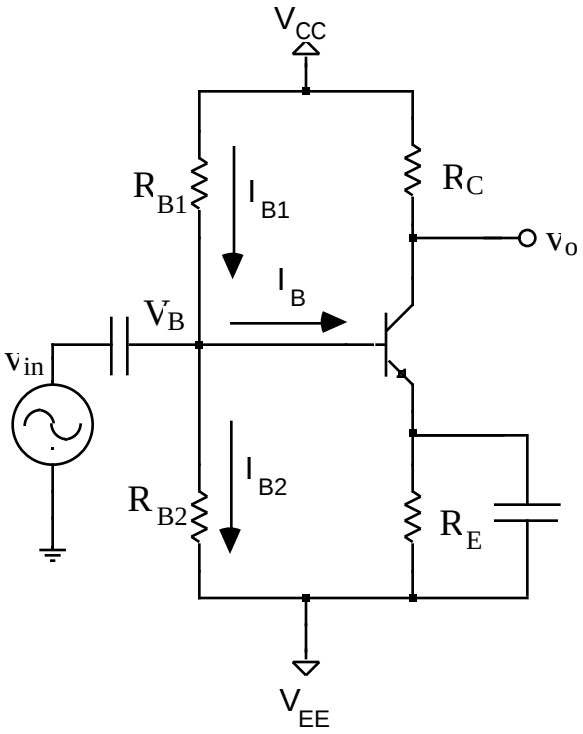
• A potential problem here is that you have an overall gain that is a function of ß!

• You cannot control that (unless you make your own transistors, and then only somewhat) and it varies with temperature!

• To get around that, you can make sure the other terms in the input voltage divider "dwarf out" R_S... in this example, if a smaller I_C were used, g_m would fall and r_π would increase to help accomplish this (of course, gain would also fall unless R_C were increased to compensate).

• It turns out that a potentially bigger problem is that g_m varies with I_C which varies with ß!... that can be fixed using a better biasing scheme...

4: CLASSIC BIASING SCHEME FOR CE AMPLIFIERS



• Typical V_{CC} = +12 or +15 V, typical V_{EE} = 0, -12V, or -15 V

5: BASE CIRCUIT DESIGN STRATEGY - THE BASICS

• It is necessary to keep V_B more than one diode drop below V_C even at maximum signal swing to prevent saturation. The method presented here is described in Sedra & Smith and is commonly used... *it is more of a rule of thumb than an absolute, however!*

• The basic idea is to set up the bias resistors to provide a nearly constant voltage at the base of the transistor, independent of its ß.

• As explained below, the emitter resistor, R_E, serves (through localized negative feedback) to trade some of the available gain of the circuit for stability in I_C, which in turn stabilizes g_m. If R_E is bypassed using a capacitor (as shown above, and commonly done), the AC gain is unaffected by R_E (since large bypass capacitors "become shorts" in the AC model). If R_E is not bypassed, the AC gain of the amplifier is reduced.

• Choose the overall magnitude of R_{B1} and R_{B2} to ensure that the current through them is about 10 - 20 X greater than the base current (i.e. only about 10% of the total current flowing in the base circuit is shunted to the base as I_B) to ensure bias stability.

• As a general rule, choose R_{B1}:R_{B2} ratio to set V_B around one-third of the way up from V_{EE} (or ground) to V_{CC}... this makes sure that V_B is much larger than any changes in V_{BE} expected due to temperature variation (V_{BE} decreases by 2 mV/°C).

6: LOCAL FEEDBACK THROUGH AN EMITTER RESISTOR

• As mentioned above, R_E is present in the CE circuit shown above to help stabilize it.

• The previously discussed biasing schemes (without R_E) are really not very good because:

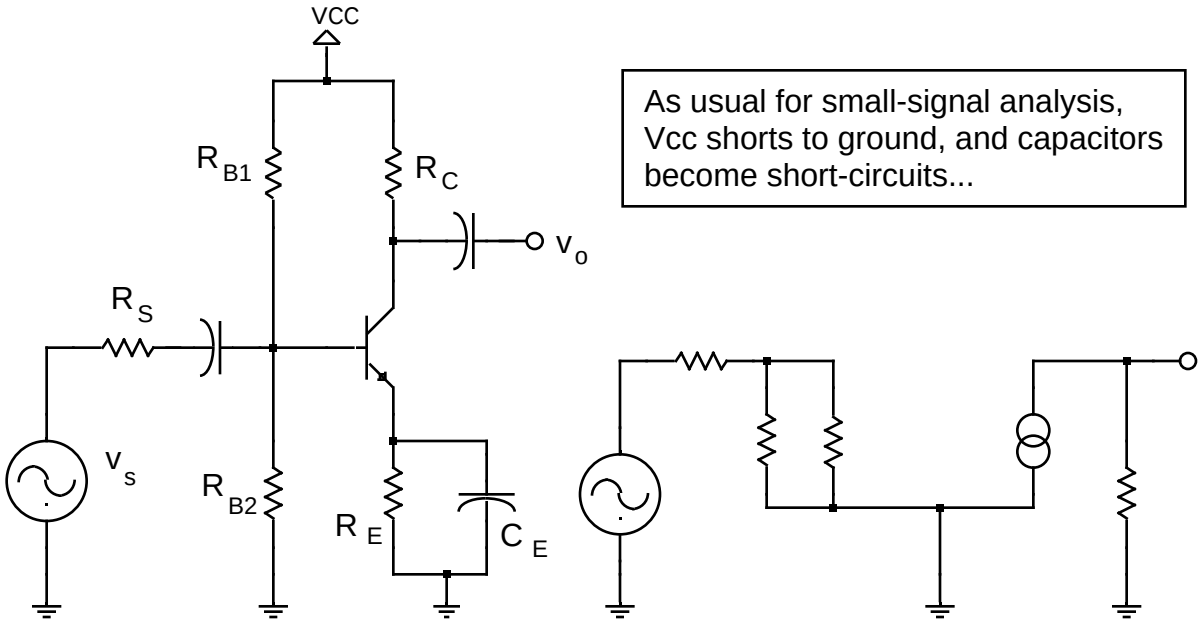
1) β varies from transistor to transistor (think about what would happen in production!)

2) g_m and β vary with I_C and temperature! Remember $g_m = \frac{I_C}{V_T}$

• **GOOD** biasing would make the bias current stable (i.e. keep I_C constant as the temperature- and device-dependent parameters changed), since variations in I_C cause variations in gain, etc.

• R_E allows for **stabilization of I_C** by feeding back an error signal if I_C increases. The error signal reduces V_{BE} enough to reduce I_C back down to where it should be.

• In general, a *bypass capacitor*, C_E, is placed in parallel with the emitter resistance, R_E, to "short out" R_E for AC signals but not disturb R_E's effect of stabilizing the bias point (which only matters at DC). Thus, a bypassed R_E provides ***DC feedback only***.



• With R_E shunted by a large enough capacitor, this gives exactly the same gain equations as we saw without R_E...

$$v_{be} = v_s \left(\frac{R_B \| r_\pi}{R_S + R_B \| r_\pi} \right)$$

$$v_o = -g_m v_{be} R_C$$

$$A_V = \frac{v_o}{v_s} = -\left(\frac{R_B \| r_\pi}{R_S + R_B \| r_\pi} \right) g_m R_C$$

This is true as long as the bypass capacitor is large enough and/or the frequency is high enough!!!!

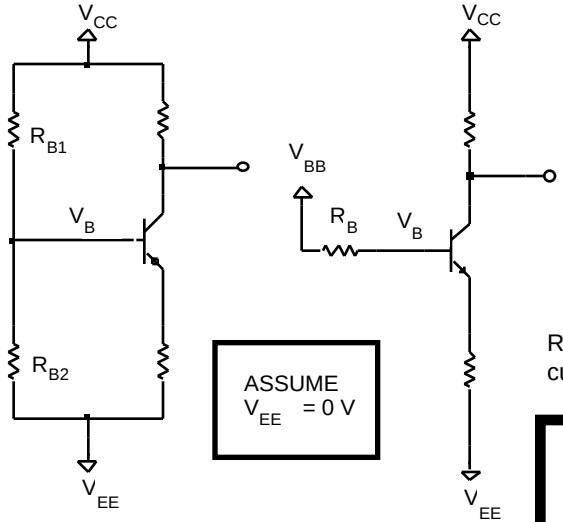
• The details of designing the whole thing, including the base circuit and R_E are presented below after some discussion of analysis and the effects of non-bypassed R_E!

7: BASE CIRCUIT ANALYSIS STRATEGY

• This section is concerned with how one analyzes the base circuit to check that it is designed correctly or to understand the operation of a circuit.

• If I_B is much smaller than the current running through R_{B1} and R_{B2}, then V_B is set by a simple voltage divider.... then one can assume a V_{BE}, compute the currents, and check the V_{BE} assumption (i.e. is the transistor in active mode versus cut-off or saturation).

• Otherwise use a **Thévenin equivalent** for the input circuit and solve the loop equation to compute I_B (see below).



Clearly $V_B = V_{BB}$ if the base current is zero! Then you just have a voltage divider.... The equivalent resistance R_B is useful to understand how the base voltage drops if the base current goes up.

Rule of thumb: this is a good approximation when the base current is <10% of the total base-circuit current...

$$V_{BB} = V_{CC} \frac{R_{B2}}{R_{B1} + R_{B2}} \qquad R_B = R_{B1} \| R_{B2}$$

Assuming $V_{EE} = 0$

BIAS CIRCUIT ANALYSIS: SEE SEDRA & SMITH EXAMPLE 4.21

• Do the example two ways...

1) Assume I_B is small relative to the total current through the bias resistors and use a simple voltage divider to compute V_B...

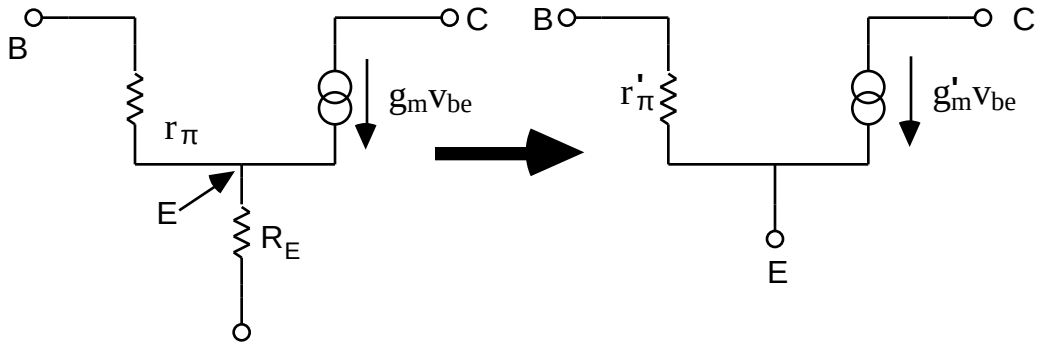
2) Do not assume anything....

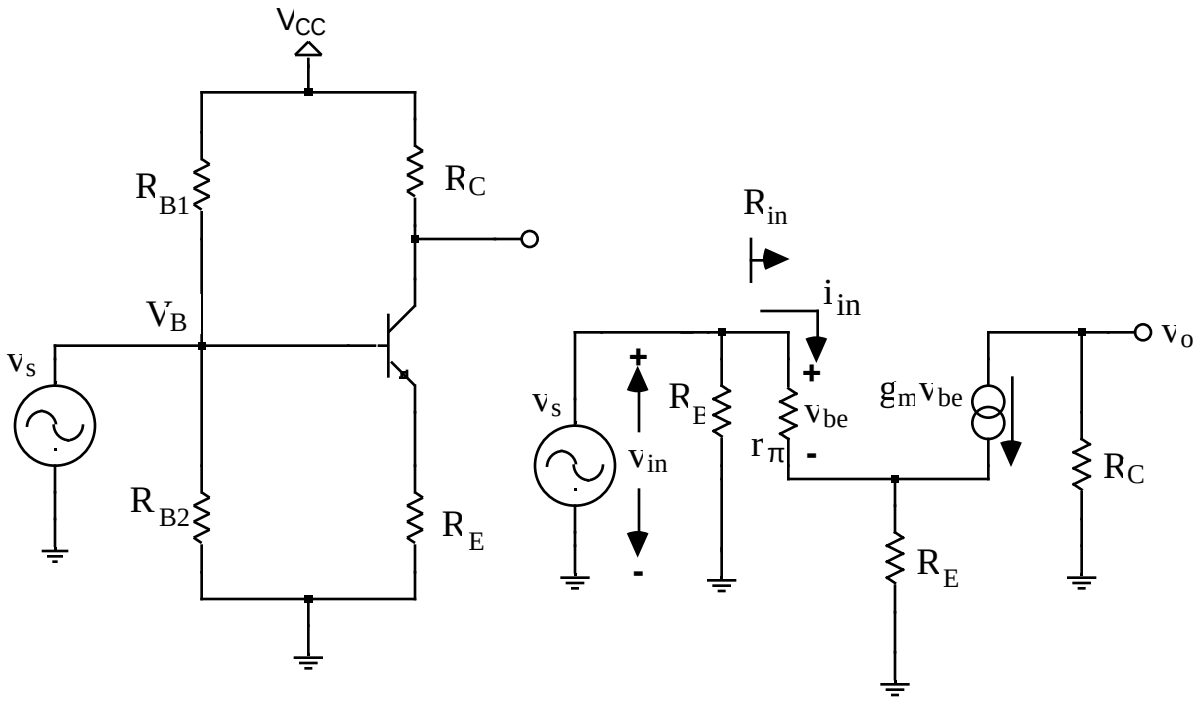
COMPARE THE RESULTS! -> The point is that if you assume a simple voltage divider, *the base current must be small relative to the current through the bias resistors!*

8: UN-BYPASSED EMITTER RESISTANCE FOR AC AND DC FEEDBACK

• With R_E not bypassed, the situation is changed so that there is a resistance from the emitter of the hybrid-π model to ground (i.e. the AC model *IS* affected by R_E).

• You can cleverly handle this by "pulling" R_E into the hybrid-π model and re-defining g_m and r_π as g_m' and r_π'... this makes the overall circuit analysis much simpler, since we can re-draw the AC equivalent circuit with the emitter of the hybrid-π model grounded, avoiding the need to write loop equations!





SIMPLIFYING ASSUMPTIONS / OBSERVATIONS:

• Ignore the source resistance R_S (not shown above) for the analysis.

• Ignore the transistor's output resistance r_o which would be in parallel with the g_m current generator....

• Take note of the fact that the (ideal) signal source is directly driving R_B, so it does not enter into our calculations...

• Calculate the **gain** and **input resistance** and compare to CE amp without R_E...

$$v_{in} = v_{be} + \left(\frac{1}{r_\pi} + g_m\right) v_{be} R_E$$ **(the second term is the voltage across R_E)**

sum of conductances seen looking into base terminal

• The other way to get this equation is from the base current,

$$v_{in} = v_{be} + (1 + \beta)\, i_{in} R_E = v_{be} + (1 + \beta)\, i_B R_E$$

$$v_{in} = v_{be} + \underbrace{(1 + \beta)\frac{v_{be}}{r_\pi}}_{i_e} R_E = v_{be} + \left(\frac{1}{r_\pi} + g_m\right) v_{be} R_E$$

• Solve for v_{be} ...

$$v_{be} = \frac{v_{in}}{1 + \left(\frac{1}{r_\pi} + g_m\right) R_E} \approx \frac{v_{in}}{1 + g_m R_E}$$

$$i_{in} = \frac{v_{be}}{r_\pi} = \frac{v_{in}}{r_\pi + \left(1 + g_m r_\pi\right) R_E} \approx \frac{v_{in}}{r_\pi\left(1 + g_m R_E\right)}$$

• Therefore, one can now **re-define the input resistance of the transistor** "taking into account" R_E,

$$R_{in} \equiv \frac{v_{in}}{i_{in}} = r_\pi + \left(1 + \beta\right) R_E \approx r_\pi\left(1 + g_m R_E\right) \equiv r'_\pi$$

• Similarly, one can look at the gain,

$$v_o = - g_m v_{be} R_C$$

• Substituting in $v_{be} \approx \frac{v_{in}}{1 + g_m R_E}$, we can **define a new g_m** "taking into account" R_E,

$$v_o = -R_c\left(\frac{g_m}{1 + g_m R_E}\right) v_{in}$$

this term is defined as g'_m

• Finally, plugging into the original CE amplifier gain equation,

$$A_V = \frac{v_{out}}{v_{in}} = -g'_m R_C = -\left(\frac{g_m}{1 + g_m R_E}\right) R_C \approx -\frac{R_C}{R_E} \quad \text{if } g_m R_E >> 1$$

• Thus, one can effectively replace the original hybrid-π model with a new one with an INCREASED r_π (now called r_π') and a DECREASED g_m (now called g_m')....

$$r_\pi' \equiv r_\pi\left(1 + g_m R_E\right)$$

$$g_m' \equiv \frac{g_m}{1 + g_m R_E}$$

• If the input divider losses are significant, they should be included in the gain equation as shown below,

$$A_V = \frac{v_{out}}{v_{in}} = -\left(\frac{R_B \,\|\, r_\pi'}{R_S + R_B \,\|\, r_\pi'}\right) g_m' R_C = -\left(\frac{R_B \,\|\, r_\pi'}{R_S + R_B \,\|\, r_\pi'}\right)\left(\frac{g_m}{1 + g_m R_E}\right) R_C$$

$$\approx -\left(\frac{R_B \,\|\, r_\pi'}{R_S + R_B \,\|\, r_\pi'}\right)\frac{R_C}{R_E} \quad \text{if } g_m R_E >> 1$$

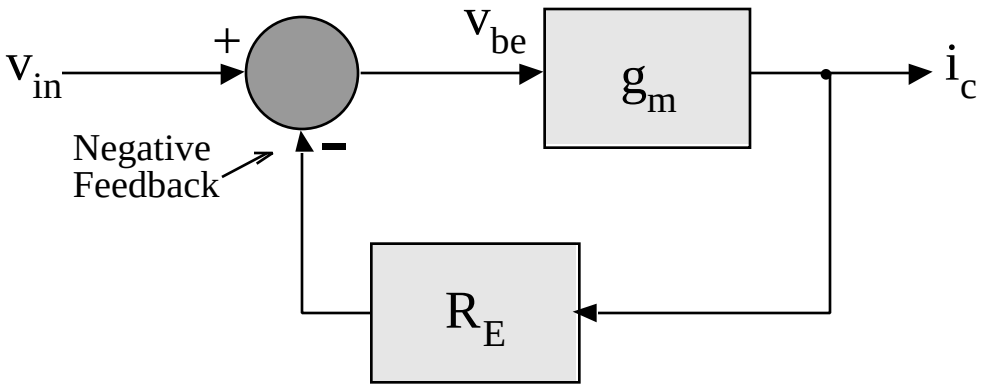
• The g_m' equation should look like the feedback equation, because that is exactly what it shows...

$$g_m' \equiv \frac{g_m}{1 + g_m R_E}$$

$$\text{GAIN} = \frac{A}{\text{AMOUNT OF FEEDBACK}} = \frac{A}{1 + A\beta}$$

• What this means is that, treating the transistor as a transconductance amplifier, we are cutting down its "open loop" transconductance g_m by a factor $(1+g_m R_E)$.

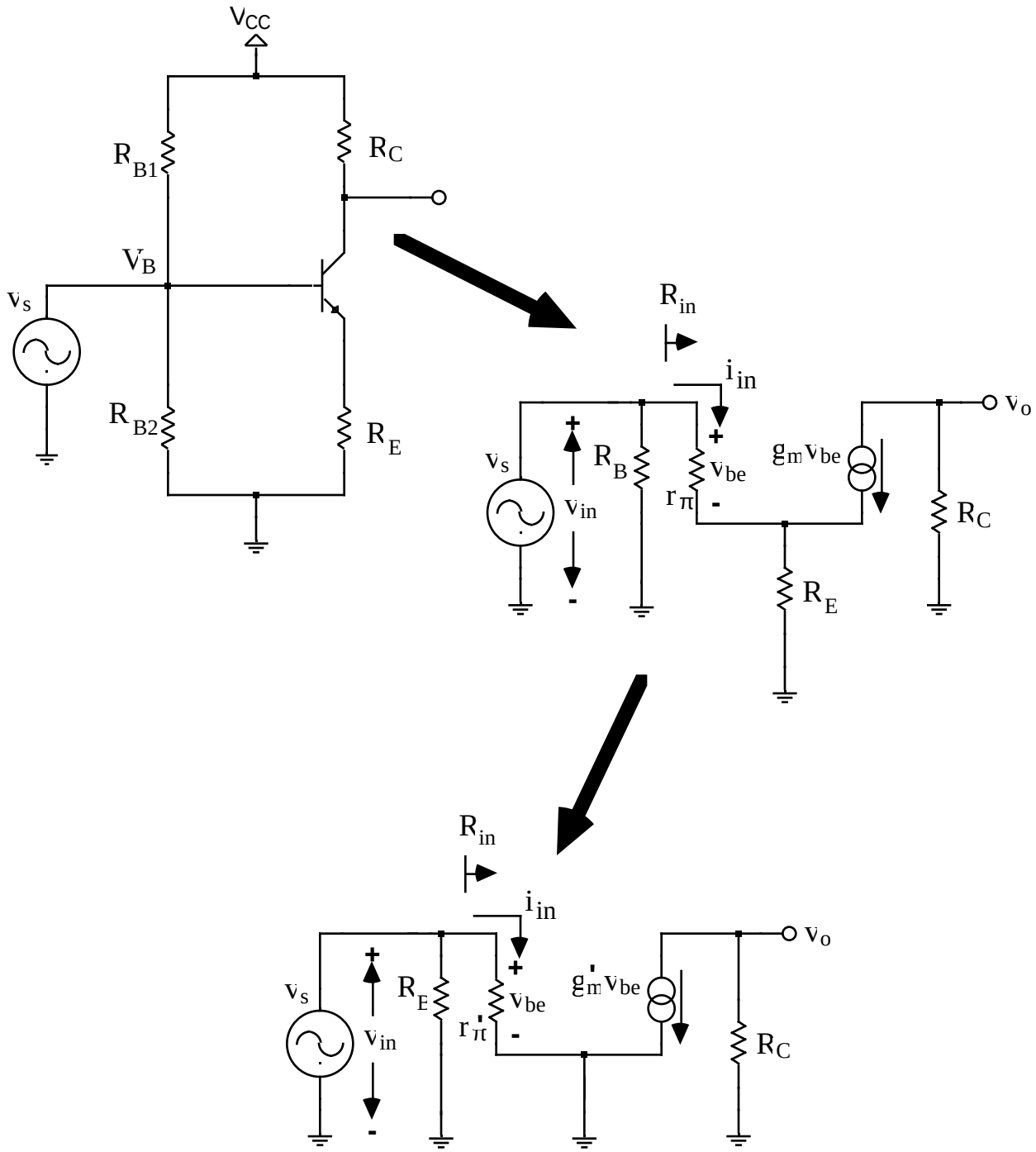
• The feedback situation for this circuit is illustrated conceptually below:



• Later in the notes, the tools to handle general feedback cases are presented.

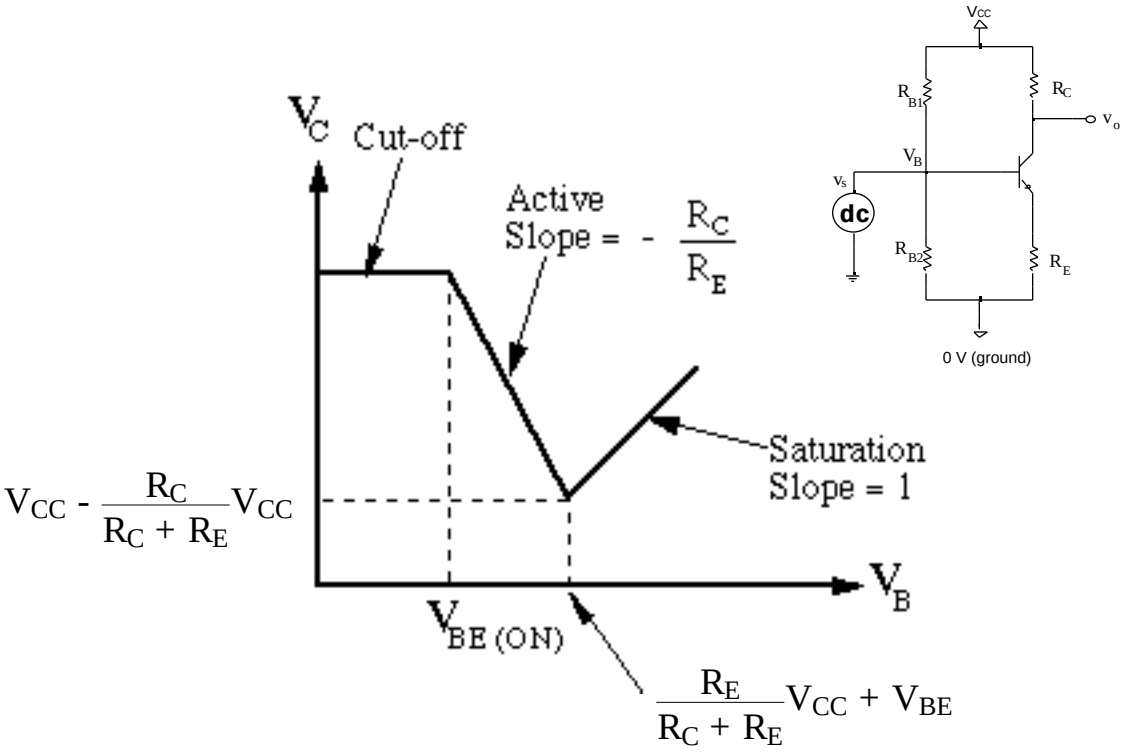
• The same approach works if you have an ***IMPEDANCE*** in the emitter circuit instead of a resistance.

• It usually makes sense to use the simplifying assumption up front, to simplify the AC equivalent circuit, the gain of which is then obtained using the standard equation for the common emitter amplifier.

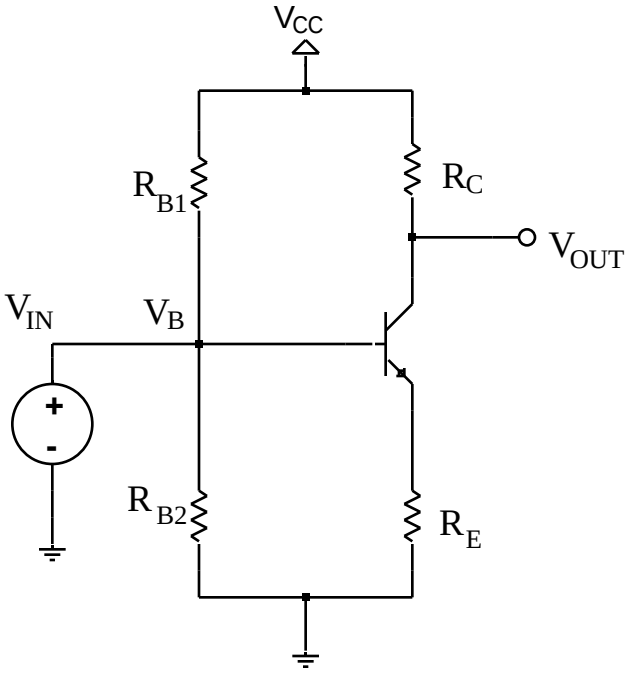

VCC
RB1
RC
VB
vs
RB2
RE
Rin
iin
vo
vs
RB
vbe
gmvbe
vin
rπ
RC
RE
Rin
iin
vo
vs
RE
gm'vbe
vbe
vin
rπ'
RC

9: EMITTER DEGENERATION

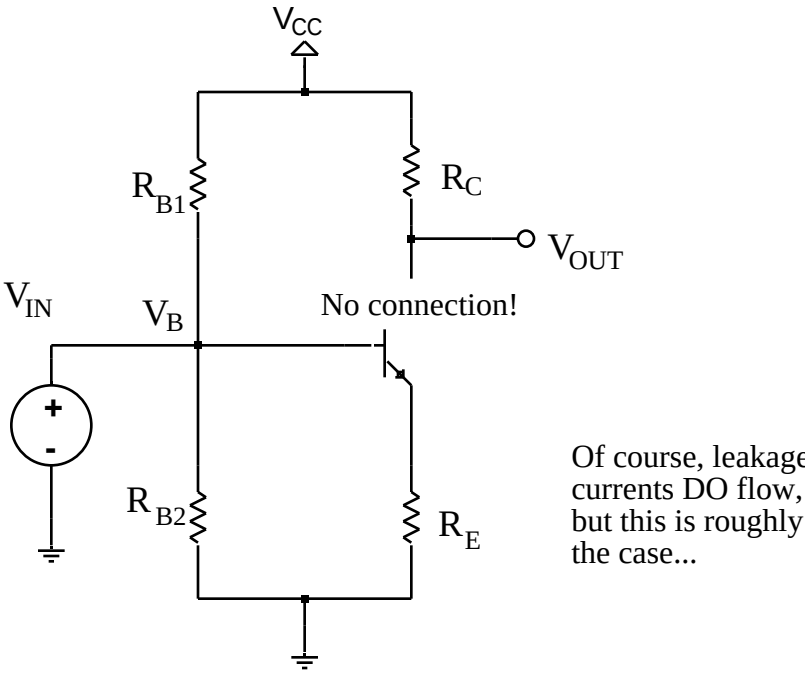
• "Emitter degeneration" describes what happens to the DC transfer function of a CE amplifier that has an un-bypassed R_E.... (note that in the active region, the slope is $-R_C/R_E$ if $g_mR_E>1$)



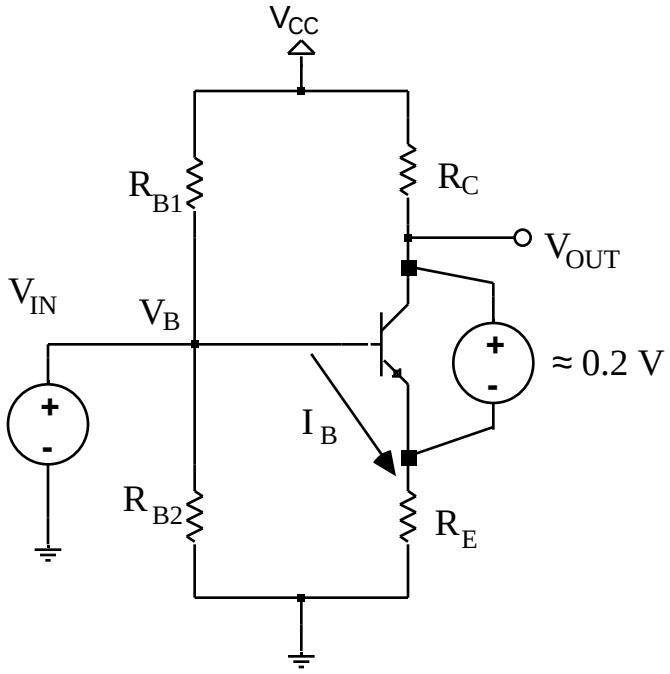
• Looking at the circuit, we can see the three cases much more clearly... For **active mode**, it looks like this:



• For **cut-off**, the circuit looks roughly like this:



• For **saturation**, the circuit looks like this:



• V_{CE} becomes V_{SAT} (which is roughly 0.2 - 0.3 V in practice) when the transistor saturates...

• The transistor is now delivering the maximum I_C it can, so I_C remains at I_{CSAT}

• Further increases in I_B simply go **directly** to the emitter circuit, **raising** V_E

• Because V_{CE} is now fixed at V_{SAT}, raising V_E ends up raising V_C (V_{OUT})

• This means that as V_B (V_{IN}) goes up, V_E just tracks it, after losing a forward biased junction drop $V_{BE(SAT)}$ which is between 0.7 and 0.8 Volts.

• That last point **explains why the slope of the transfer function becomes one in saturation...** the input voltage V_B is essentially shorted to V_E, which is essentially shorted to V_{OUT}!

• This means that V_{OUT} just tracks further increases in V_{IN} (certainly, if V_{IN} is an ideal voltage source, it can drive V_{OUT} just fine!).

• Of course, when saying things are "shorted," it is assumed that we can ignore the small voltage drops (0.7 V between B and E, and 0.2 V between C and E).

• Note that with 0.2 V between collector and emitter, the BC junction voltage is actually about 0.5 V, so the BC junction is not fully forward biased. Also, the extra base current flowing into the transistor does not flow out the collector because it is at a higher potential than the emitter!

• Now it is worthwhile to modify our previous Spice deck (our design example) for time-domain analysis and put in a single cycle of a BIG sinewave (7 V!) to look at what happens when the amplifier hits the limits of its voltage transfer function (cutoff and saturation)...

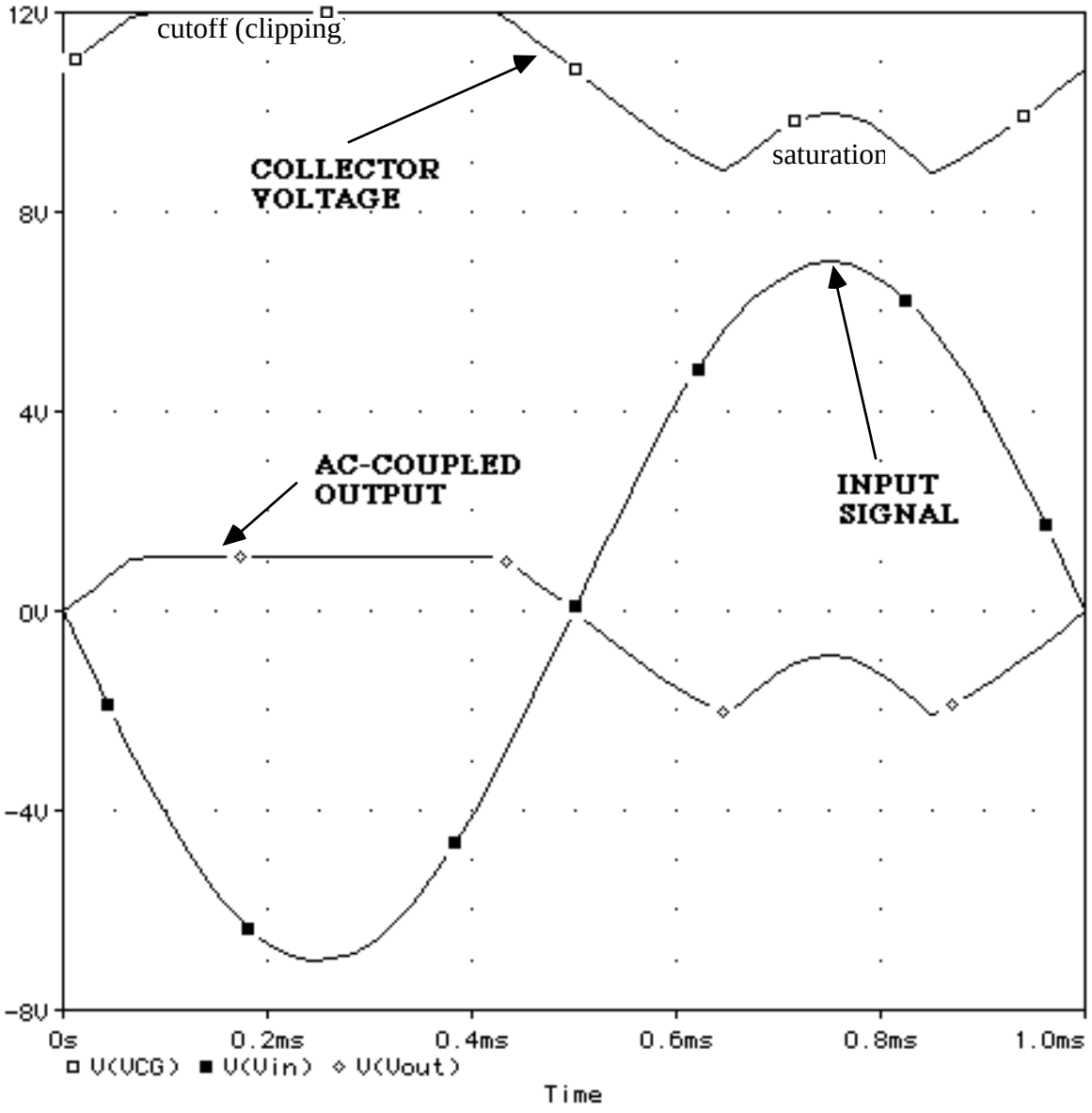
```
EE113 Example Degenerated Common-Emitter Amplifier
*dc components
Vcc VCC   0          12
R1  VCC   VBG        39K
Q1  VCG   VBG   VEG  TRANSMODEL
R2  VBG   0          18K
RC  VCC   VCG        680
RE  VEG   0          1.8K
*.MODEL TRANSMODEL NPN (IS=1.3E-14)

*ac components
Vss 0     Vin        sin(0 7 1000)
RS  Vin    VX        1
C3  VX    VBG        100UF
*C6  VEG   0          100UF
C5  Vout  VCG        100UF
RLL Vout  0          50K
.MODEL TRANSMODEL NPN (BF=150 IS=1.3E-14
+ TF=.9N  CJE=6P  CJC=5P)
*Time Domain Response
.TRAN 100nS 1mS
.PROBE
.end
```

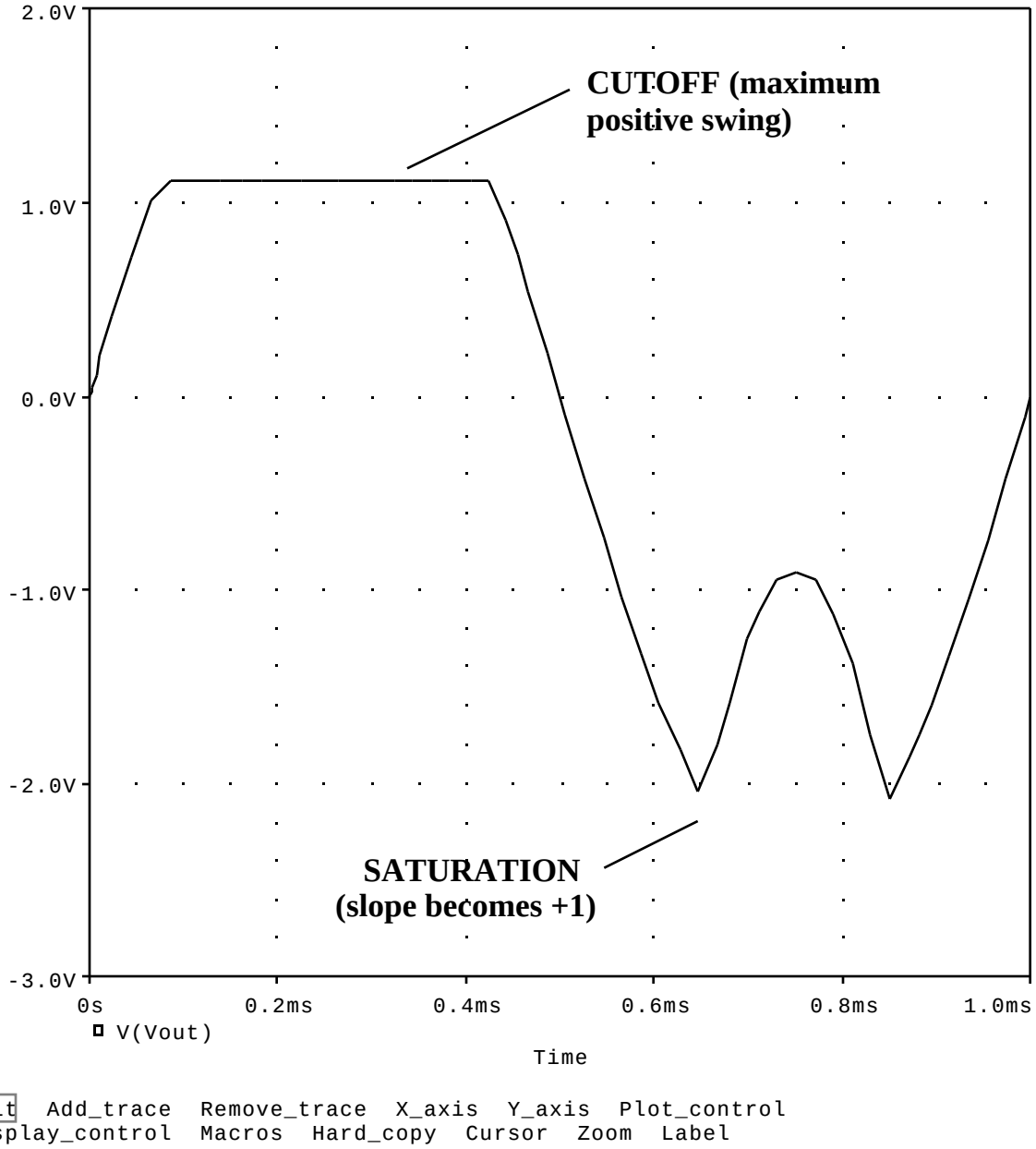
The asterisk in front of this line removes the bypass capacitor from across R .....

• Here is the result, showing input and output signals...

NOTE THAT THE SPICE DECK CONTAINS AN ***OUTPUT COUPLING CAPACITOR*****, which explains why the AC-coupled output is centered around 0 V while the collector voltage si swinging near to + 12 V!**



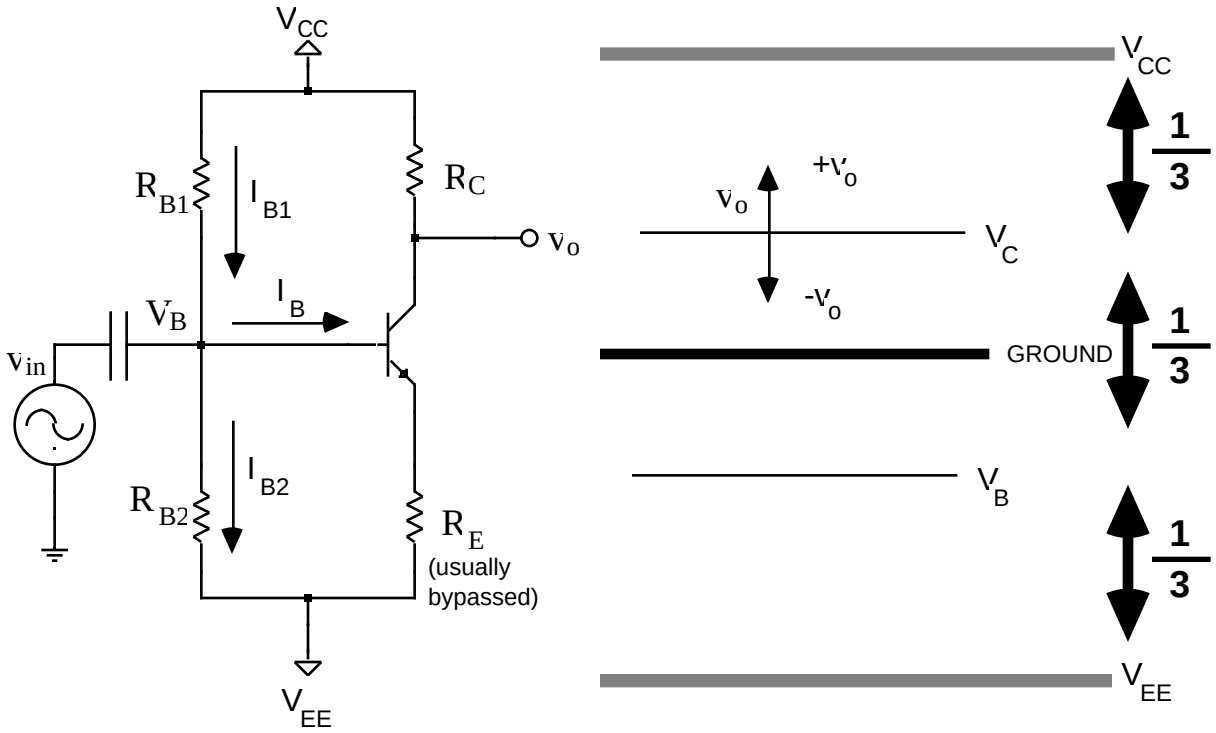
• Below is an expanded view of the output signal (AC-coupled)...



• Now you can see why we bother looking at the transfer function... it predicts the kind of distortions you see when you over-drive an emitter-degenerated (un-bypassed R_E) common-emitter amplifier.

10: THE BOTTOM LINE ON DESIGN OF CE AMPLIFIERS

• Typically you design to meet a power dissipation specification (i.e. the maximum I_C tolerable for a reasonable battery life...) and want maximum output signal swing... let's go through the thinking behind it and then a design example using the methods of Sedra and Smith.



• Typical V_{CC} = +15 V, typical V_{EE} = -15 V (other common voltages = +/- 12 V)

• The rule of thumb approach is to design for the voltage between the power supplies to be split (roughly) into thirds....

$$V_B = \frac{1}{3}\left(V_{CC} - V_{EE}\right)$$

$$V_C \approx \frac{2}{3}\left(V_{CC} - V_{EE}\right)$$ NOTE that this is not a design constraint!

Note that the V_C value specified is the *quiescent* (no input signal) value). ***Do not*** *try to force it to that value.* V_C may be considerably lower if the current (and gain) is increased.

1) Assuming that you know the desired DC collector current, you compute the resistor values (for DC) that give you this current.

2) Then choose the bias resistors R_{B1} and R_{B2} so that the 1/3 rule is obeyed and so that the base current is in the range $I_B \approx 0.1\ I_{B1}$ so that the "voltage divider" assumption is reasonably close (i.e. the base current doesn't change V_B much).

Rules of thumb for this are:

$V_{BB} >> V_{BE}$ This ensures that small variations in V_{BE} (near 0.7V) will be dwarfed by V_{BB} being so much higher so that I_B will not change much...

Remember that $I_E = \frac{V_{BB} - V_{BE}}{R_E}$

$R_E >> \frac{R_B}{(\beta + 1)}$ This ensures that R_E is large enough to provide adequate local feedback to stabilize I_E (and hence, I_C)... The term on the right is simply the Thévenin equivalent of the bias resistors as "seen" from the emitter (remember that dividing by (β + 1) "transforms" resistances from the base circuit to the perspective of the emitter circuit).

11: THE ART OF CE DESIGN (AN INTRO)

• Which ever approach you take to designing CE amplifiers, you will typically be designing them to meet certain specifications, such as gain, power dissipation (quiescent), specific collector (or emitter current), etc.

• The approach you take depends on which of these specifications are given and which are most important.

• For example, **if the gain was specified**, you would probably start with the voltage gain equation for the configuration you wish to use to get a feel for the constraint. The equation for the case where R_E is bypassed is,

$$A_v = \frac{v_o}{v_s} = -\left(\frac{R_B \,||\, r_\pi}{R_S + R_B \,||\, r_\pi}\right) g_m R_C$$

and for when R_E is *not* bypassed,

$$A_V = \frac{v_{out}}{v_{in}} = -\left(\frac{R_B \,||\, r'_\pi}{R_S + R_B \,||\, r'_\pi}\right) g'_m R_C = -\left(\frac{R_B \,||\, r'_\pi}{R_S + R_B \,||\, r'_\pi}\right)\left(\frac{g_m}{1 + g_m R_E}\right) R_C$$

$$\approx -\left(\frac{R_B \,||\, r'_\pi}{R_S + R_B \,||\, r'_\pi}\right)\frac{R_C}{R_E} \quad \text{if } g_m R_E >> 1$$

• You then look to see what determines the gain. In this case, if $g_m R_E >> 1$, it is purely the ratio of the resistances (neglecting the effects of the input divider)....

$$A_v \approx - \frac{R_C}{R_E}$$

• For a **non-degenerated** CE amplifier (R_E bypassed by a large enough capacitor), the gain is $-g_m R_C$, so you need to be careful to set g_m to an appropriate value by choosing I_C, knowing that,

$$g_m = \frac{I_C}{V_T}$$

If R_E is bypassed, you can adjust its value to control I_C and hence gain.

• This is where your design begins in this case, with the collector emitter circuit, followed by the design of the bias circuitry.

• If you have a power constraint, you typically start by determining the maximum allowable collector current, and hence the maximum available gain.

Typically, you would derive exact component values using a design method you choose (see below), substitute the nearest "real" component values, and simulate the circuit using SPICE before building a prototype.

• You may need to consider the effects of **load resistances** on the overall gain. For capacitively-coupled amplifiers, these loads do not affect the bias point.

• At this point we won't worry much about designing to take into account the frequency response of the BJT amplifier (this is covered below).

REMINDER: You should always remember these relationships (they are very handy and we use them below!).

$$I_E = (\beta + 1) I_B \quad \text{and} \quad I_B = \frac{I_C}{\beta}$$

thus,

$$I_E = \left(\frac{\beta + 1}{\beta}\right) I_C$$

(That makes sense because I_E is larger than I_C...)

12: BIAS CIRCUITRY DESIGN

• Try to choose R_{B1} and R_{B2} so that I_B is small compared to the current flowing through R_{B1} and R_{B2}...

• To select R_B for bias stability (resistant to changes in β and temperature, T), a rule of thumb is to set the bias network (R_{B1} and R_{B2}) up so that approximately 10% of the total current through R_{B1} and R_{B2} goes into the base of the transistor.

• Sedra and Smith suggest a rule of thumb for selecting the bias resistors that is to set the voltage divider current to 0.1 I_E.

• So, if you have I_E, you can do it directly.

• If you don't, you can calculate I_E from I_B...

$$I_{BIAS} \approx \frac{V_{CC}}{R_{B1} + R_{B2}} = 0.1\ I_E = 0.1\ (1 + \beta)\ I_B$$

• To set V_B at roughly 1/3 of the supply voltage, you can write...

$$\frac{1}{3} = \frac{R_{B2}}{R_{B1} + R_{B2}} \qquad \text{...this is} \quad \frac{1}{3}(V_{CC} - V_{EE}) = \frac{R_{B2}}{R_{B1} + R_{B2}}(V_{CC} - V_{EE})$$

• Combining these, you get,

$$R_{B2} = \frac{V_{CC}}{0.3\ I_E}$$

and

$$R_{B1} = \frac{V_{CC}}{0.1\ I_E} - R_{B2}$$

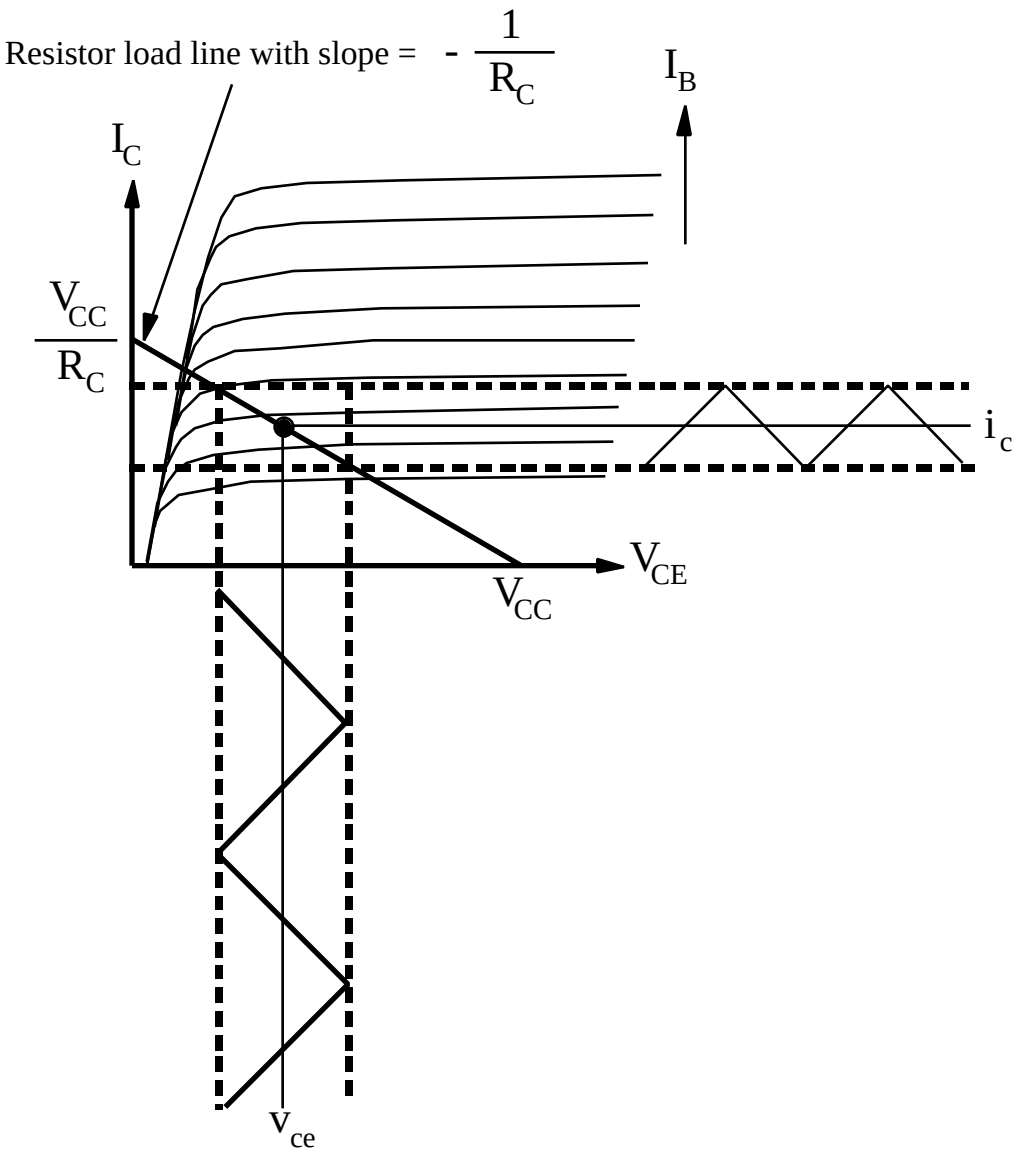
• Substitute V_{CC}-V_{EE} for V_{CC} in the above equations if dual power supplies are used.

13: REVISITING LOAD LINES

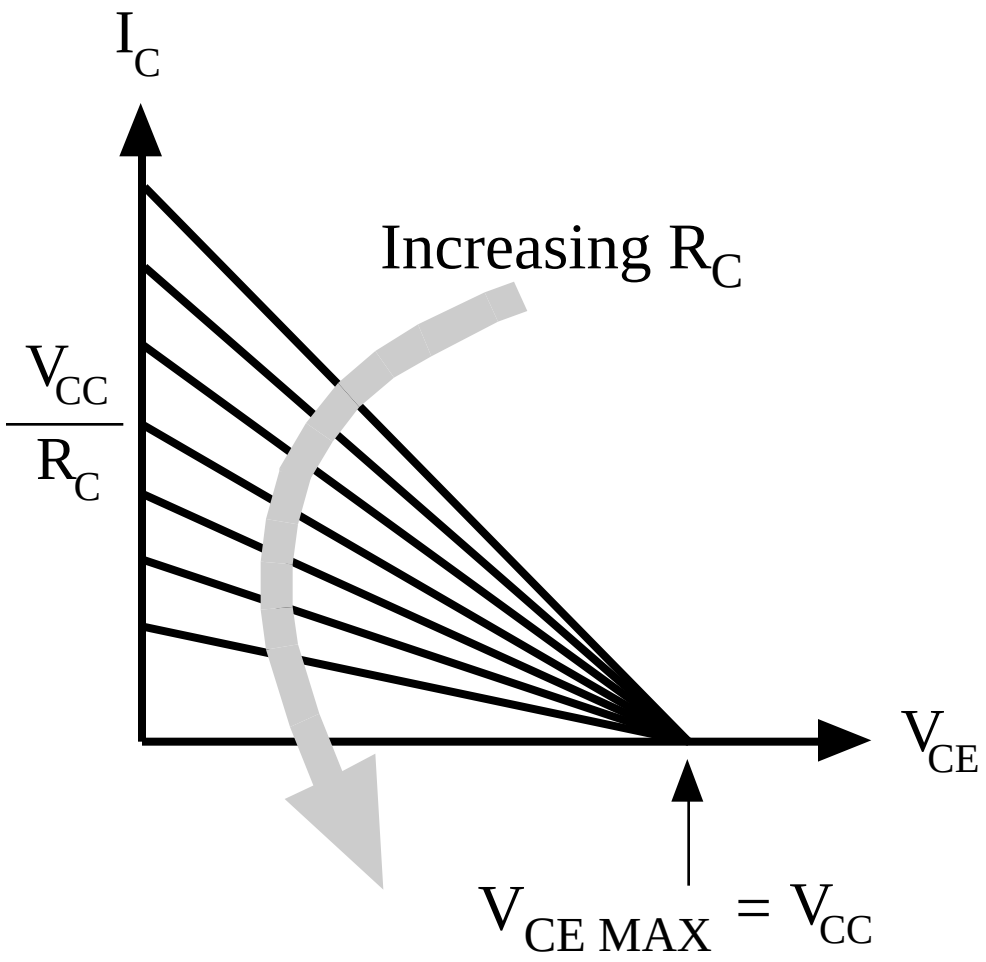
• The load line approach lets us solve two simultaneous equations: **1) the I_C versus V_{CE} curve of the BJT** (remember that only particular curves are plotted for specific I_B values, but effectively there are an infinite number of them... it is really a 3D plot) and **2) the resistor's I_C versus V_{CE} line due to the collector resistor** (Ohm's Law).

• "Wiggling" the base current moves you up and down along the constraint of the resistor load line, generating a corresponding output "wiggle" in v_{ce} and consequently v_{out}!

• NOTE that here we assume a simple CE amplifier (no R_E), so $V_{CE} = V_C$.



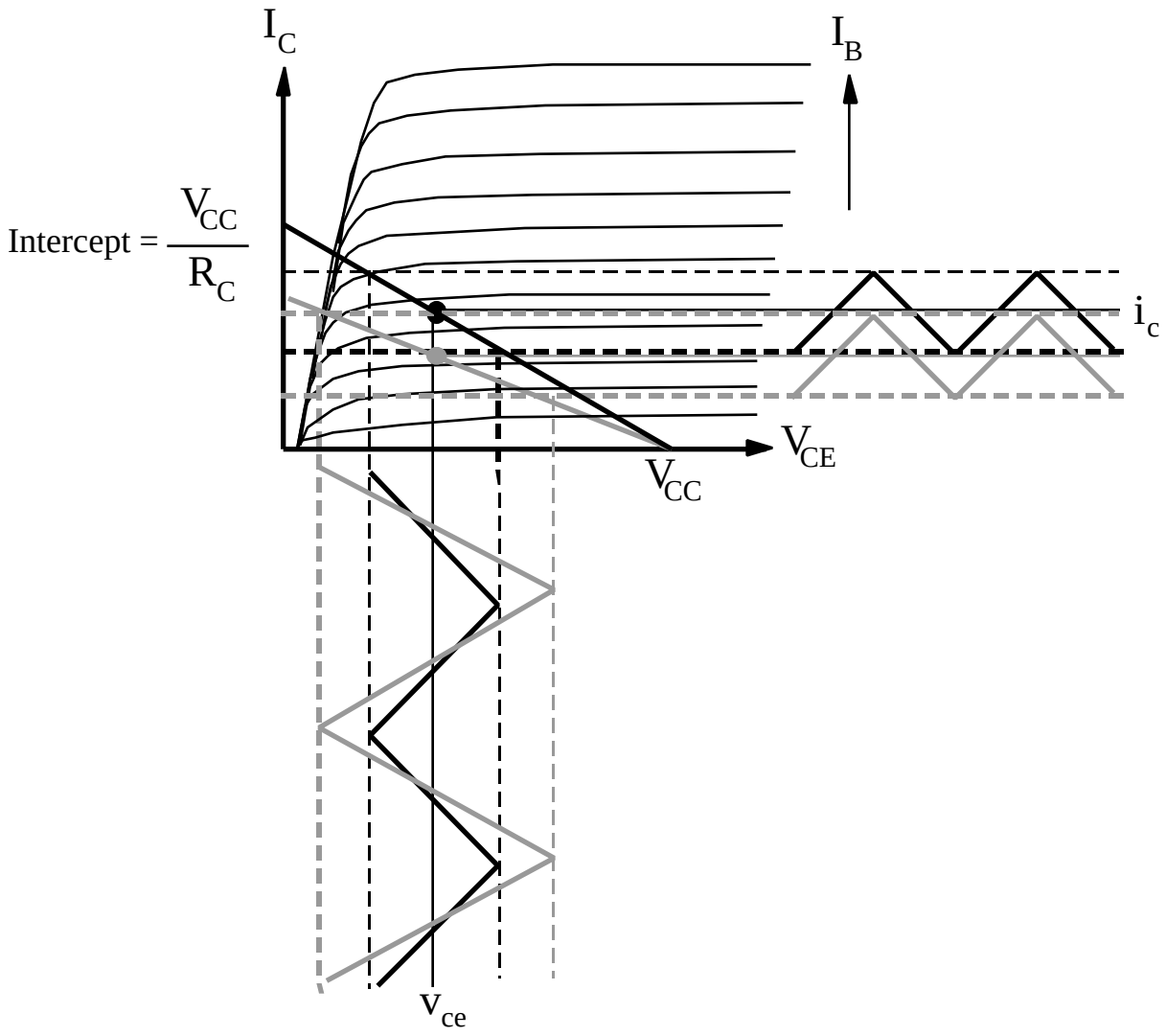
• The slope of the resistor load line controls the gain - **the larger R_C, the shallower the slope of the line and the larger the output signal swing...**



• This helps explain the effect of R_C on the gain of the simple CE amplifier, where,

$$A_V = -g_m R_C$$

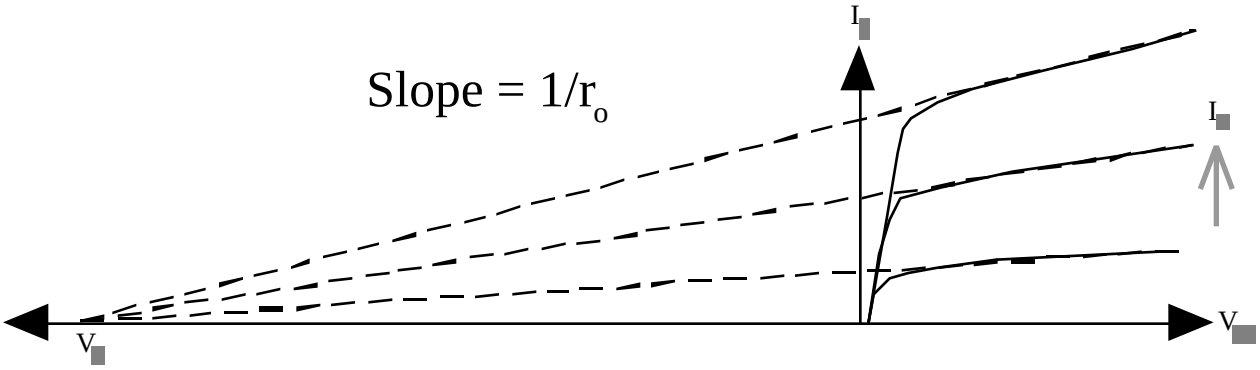
• Combining two resistive load lines into one (somewhat crowded) plot helps bring it together.



• **Note that g_m is effectively set by the quiescent-point (no signal current, or Q-point) current!!!...** moving to a lower Q-point also decreases gain... what is not illustrated by the simple load line drawings here is that the slopes of the V_{CE} versus I_C curves for the BJT increase with increasing I_C.

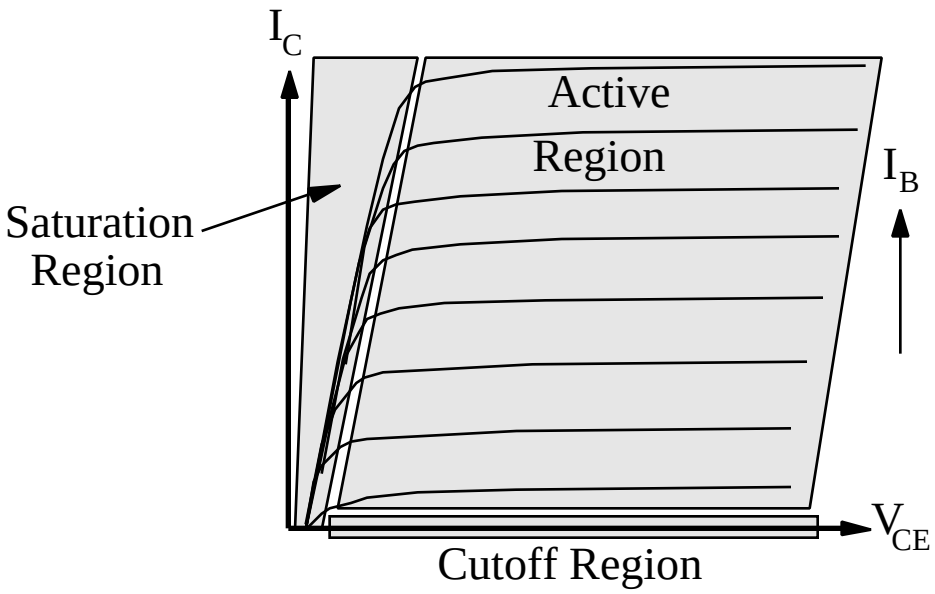
• The **Early Voltage**, discussed later on with respect to BJT current sources, represents an effective output resistance, r_o, between the collector and emitter... this gives rise to the **gradually increasing slope of the I_C versus V_{CE} curves for increasing I_C** (see pages 207 - 208 in S & S).

$$r_o = \frac{V_A}{I_C}$$



• Remember that in the above figure, the I_C versus V_{CE} curves represent equal base current steps between them.

• If I_C is increased to increase g_m, the DC collector voltage, V_C, will come closer to ground (i.e. V_{CE} will decrease) **until the transistor is saturated**.



• This means that, for a given supply voltage, there is a limit to the amount of gain one can get from a given transistor and power supply voltage... **note that the V_{CE}-intercept of the resistor load line is determined entirely by the supply voltage.**

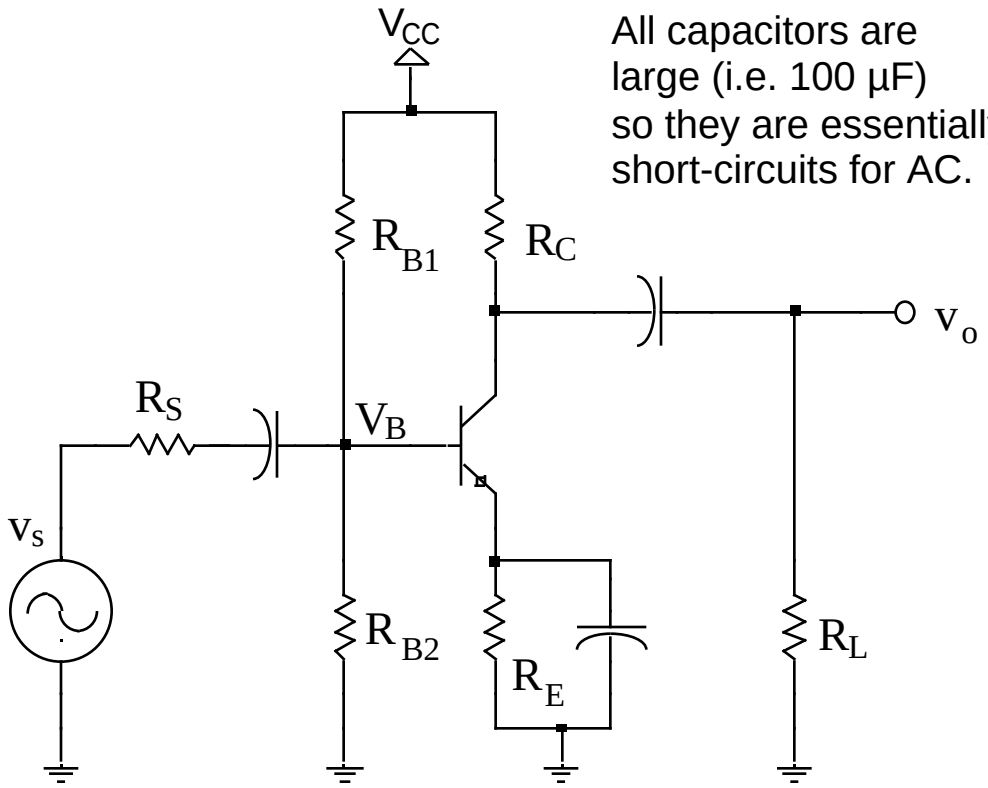
• One can solve for this maximum gain by setting V_{CE} to some minimum voltage, V_{CEmin} to allow a reasonable swing (e.g. 1 V) and observing that the gain equation for a common emitter amplifier is independent of R_C... (the input divider is ignored here),

$$A_V = -g_m R_C = -\frac{I_C}{v_T} R_C = -\frac{\left(V_{cc} - V_{CEmin}\right)}{R_C}\left(\frac{1}{v_T}\right)R_C$$

14: DESIGN EXAMPLE #1: METHOD OF SEDRA & SMITH

Specifications:

DC power dissipation: P_D < 30 mW
Power supply: 12 VDC
Voltage Gain: -50X
Load: Resistive, 50 kΩ
Assume R_s = 0 Ω
Must use 2N2222A Transistor (NPN, β = 150 measured)



We know that the total power dissipation (DC, or quiescent) and the voltage gain both are determined by the choice of current in the collector-emitter circuit.

SO, START THERE!

1) Calculate I_{max} at 30mW/12VDC = 2.5 mA

2) We know that the gain of this amplifier with R_E bypassed (shorted to ground for AC signals) is,

$$A_v = \frac{v_o}{v_{be}} = -g_m R_C$$

and that

$$g_m = \frac{I_C}{V_T}$$

In this "quick" design, we are ignoring the effects of the input voltage divider (bias resistors). This should not be done in general, since these resistors will typically reduce overall gain (unless R_S is zero).

choosing I_c = 2.0 mA, we see that g_m is,

$$g_m = \frac{I_C}{v_T} = \frac{2\text{ mA}}{25.9\text{ mV}} = 0.0772\ \Omega^{-1}$$

now we can calculate R_C (assuming R_E is fully bypassed for AC)

$$R_C = \frac{-A_V}{g_m} = \frac{50}{0.0772} = 647.5\ \Omega$$

assuming the 1/3, 1/3, 1/3 rule of Sedra & Smith, we also allow V_{CE} = 12/3 = 4V and can choose R_E by,

$$R_E = \frac{V_B - V_{BE}}{I_E} = \frac{V_B - V_{BE}}{\left(\frac{\beta + 1}{\beta}\right) I_C} = \frac{4 - 0.7}{\left(\frac{150 + 1}{150}\right) 0.002} = 1{,}639\ \Omega$$

3) Now calculate the required base current,

$$I_B = \frac{I_C}{\beta} = \frac{2\text{ mA}}{150} = 0.0133\text{ mA}$$

4) Knowing the base current, and that V_B should be 1/3 of the way up from ground to +12 V, and assuming that the current in the voltage divider is $0.1I_E$, we can calculate the bias resistor circuit,

$$R_{B2} = \frac{V_{CC}}{0.3I_E} = \frac{V_{CC}}{0.3(1+\beta)I_B} = \frac{12}{0.3(1+150)\ 13.3\,\mu A} = 19.92\ k\Omega$$

$$R_{B1} = \frac{V_{CC}}{0.1I_E} - R_{B2} = \frac{V_{CC}}{0.1(1+\beta)I_B} - R_{B2} = \frac{12}{0.1(1+150)\ 13.3\ \mu A} - 19.92\ k\Omega = 39.83\ k\Omega$$

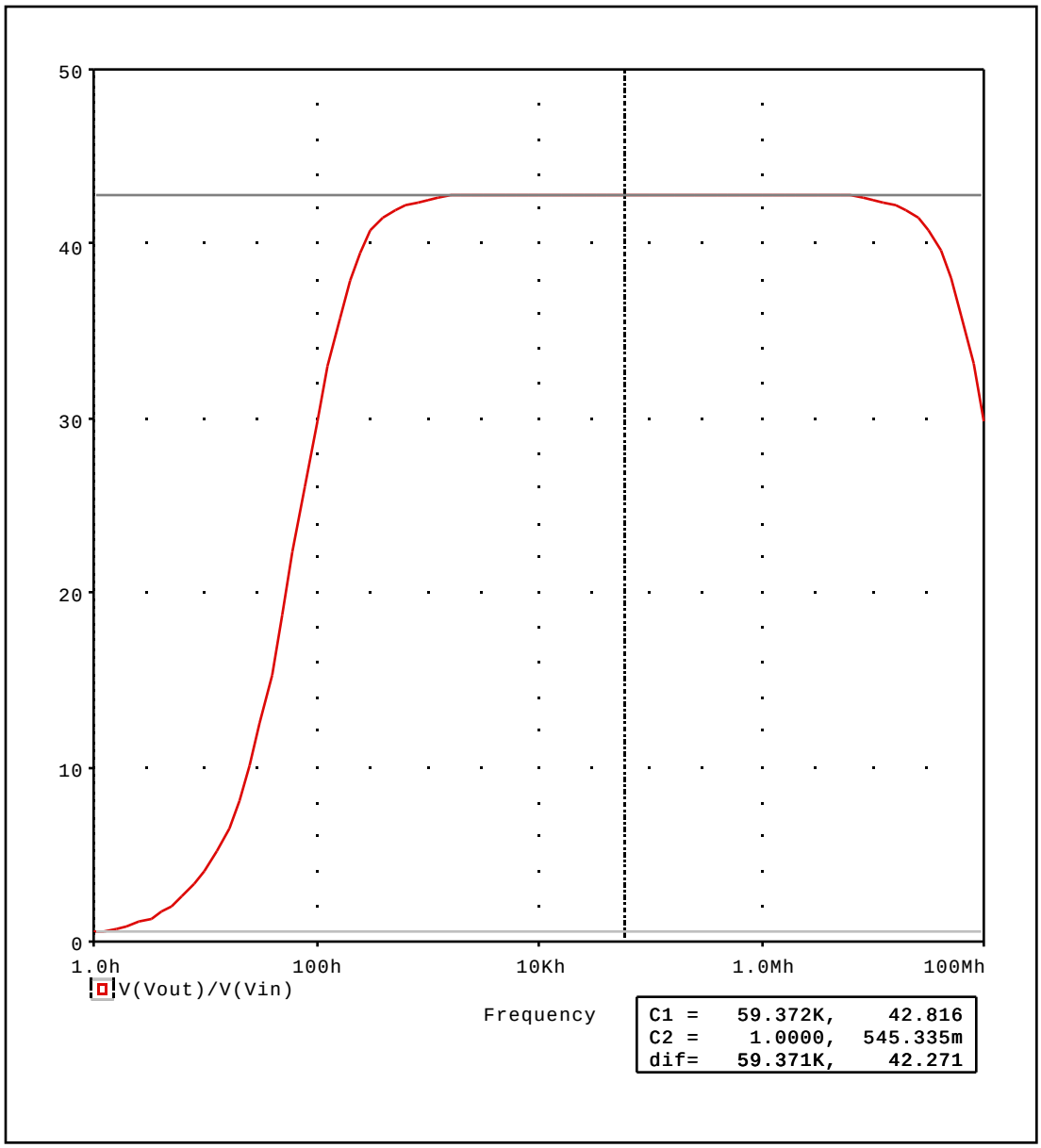
5) Choose "real" component values close to those calculated...

R_C = 680 Ω R_E = 1.8 kΩ

R_{B1} = 39 kΩ R_{B2} = 18 kΩ

6) SIMULATE the circuit using SPICE...

```
EE113 Example Design #1 Common-Emitter Amplifier
*dc components
Vcc VCC   0          12
R1  VCC   VBG        39K
Q1  VCG   VBG   VEG  TRANSMODEL
R2  VBG   0          18K
RC  VCC   VCG        680
RE  VEG   0          1.8K
*.MODEL TRANSMODEL NPN (IS=1.3E-14)
*ac components
Vss 0     Vin        AC 10mV
RS  Vin    VX        1
C3  VX    VBG        100UF
C6  VEG   0          100UF
C5  Vout  VCG        100UF
RLL Vout  0          50K
.MODEL TRANSMODEL NPN (BF=150 IS=1.3E-14
+ TF=.9N  CJE=6P  CJC=5P)
*input sweep for Bode plot
.AC DEC 10 1 100MEG
.PROBE
.end
```

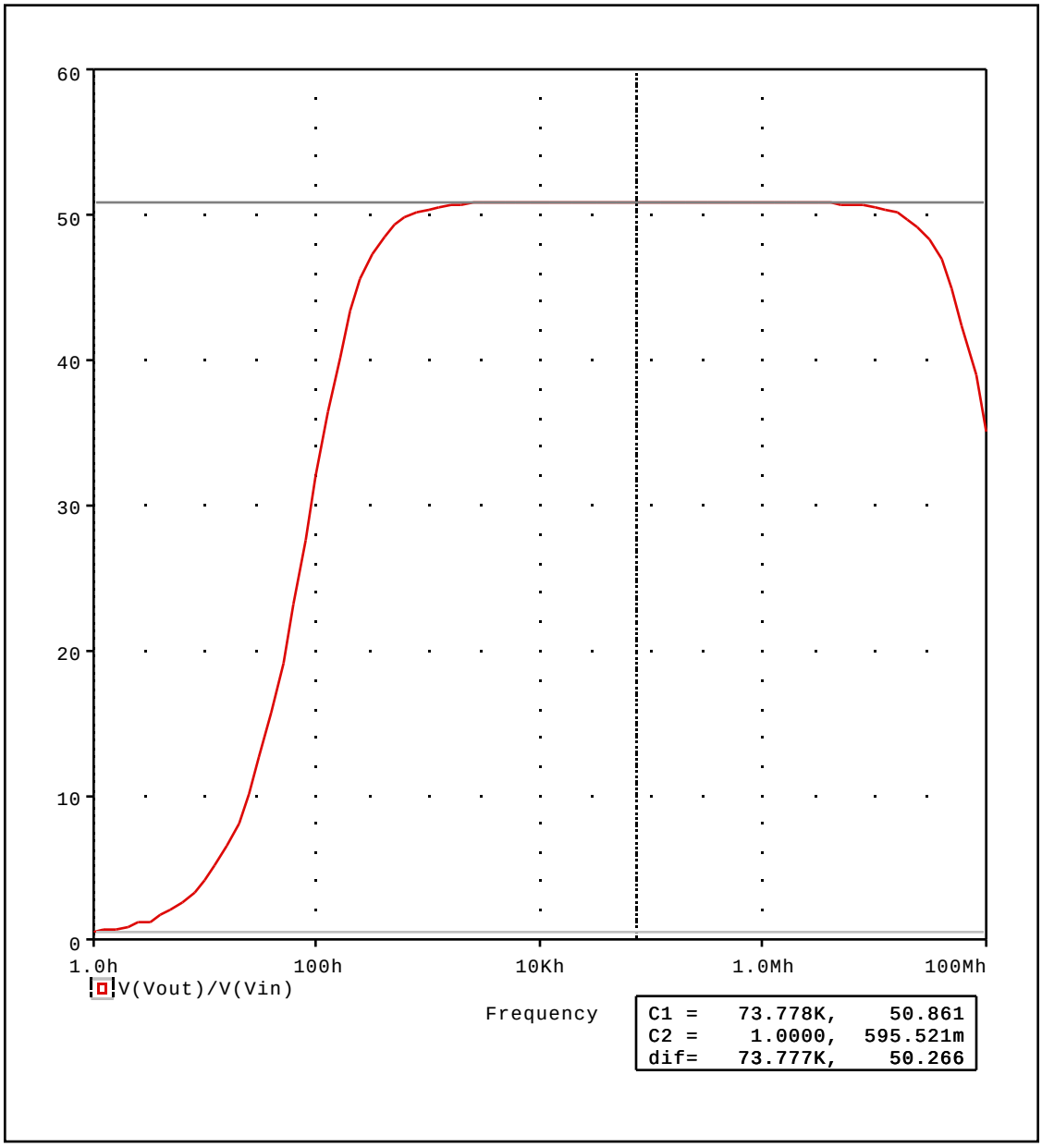


We see that the mid-band gain is only 43X !!!!

Noting that,

$$g_m = \frac{I_C}{v_T} = \frac{\left(\frac{\beta}{\beta+1}\right) I_E}{v_T} = \frac{V_B - V_{BE}}{\left(\frac{\beta}{\beta+1}\right) R_E v_T} \approx \frac{127.4}{R_E}\ \Omega^{-1}$$

we see that the gain can be directly controlled via R_E. To do this, we scale the original computed R_E (1.639 kΩ) by the ratio of the actual to desired gain (0.84) to obtain 1.41 kΩ, and choose a real valued R_E = 1.5 kΩ and simulate again....



A gain of 50.9 is probably close enough!

Checking the power drain as computed by SPICE,

```
 VOLTAGE SOURCE CURRENTS
   NAME         CURRENT
   Vcc         -2.177E-03
   Vss          0.000E+00

   TOTAL POWER DISSIPATION   2.61E-02  WATTS
```

Looks fine! Build it!

15: WHEN DOES THE INPUT DIVIDER MATTER?

• If the input divider is considered up-front in a design where $R_S \neq 0$, the power dissipation constraint in this example still is the best place to start, and we begin by choosing I_C= 2 mA, giving $g_m = 0.0772\ \Omega^{-1}$.

• Then you would refer to the "full" gain equation and note that the input divider values would need to be determined before choosing R_C,

$$-50 = A_v = \frac{v_o}{v_s} = -\left(\frac{R_B \,||\, r_\pi}{R_S + R_B \,||\, r_\pi}\right) g_m R_C$$

• Assuming the 1/3, 1/3, 1/3 rule of Sedra & Smith, we also allow V_{CE} = 12/3 = 4V and can choose R_E by (same as before),

$$R_E = \frac{V_B - V_{BE}}{I_E} = \frac{V_B - V_{BE}}{\left(\frac{\beta + 1}{\beta}\right) I_C} = \frac{4 - 0.7}{\left(\frac{150 + 1}{150}\right) 2\ \text{mA}} = 1{,}639\ \Omega$$

• Again, we calculate the required base current,

$$I_B = \frac{I_C}{\beta} = \frac{2\ \text{mA}}{150} = 0.0133\ \text{mA}$$

• Knowing the base current, and that V_B should be 1/3 of the way up from ground to +12 V, and assuming that the current in the voltage divider is $0.1I_E$, we can calculate the bias resistor circuit,

$$R_{B2} = \frac{V_{CC}}{0.3\ I_E} = \frac{V_{CC}}{0.3\ (1 + \beta)\ I_B} = \frac{12}{0.3\ (1 + 150)\ 0.0133\ \text{mA}} = 19.92\ \text{K}\Omega$$

$$R_{B1} = \frac{V_{CC}}{0.1\ I_E} - R_{B2} = \frac{12}{0.1\ (1 + 150)\ 0.0133\ \text{mA}} - 19.92\text{K}\Omega = 39.83\ \text{K}\Omega$$

• Thus far, the calculations have been the same, but the final calculation of R_C must be done differently. First, you need to compute r_π,

$$r_\pi = \frac{\beta}{g_m} = \frac{150}{0.0772} = 1943\ \Omega$$

• Here there is a choice. You can pick real values for R_{B1} and R_{B2} and solve the "full" gain equation for R_C (knowing R_S). Or, you can make the calculation using the "accurate" values and then pick "real" ones later. The first choice is usually better, since then there is only one resistor that is not accurately represented in the calculations when the nearest "real" value is chosen (R_C).

• Choosing "real" values, R_{B1} = 39 kΩ and R_{B2} = 18 kΩ. Then the gain equation can be solved for R_C (assuming R_S = 50Ω in this example),

$$R_C = \frac{-A_v}{\left(\frac{R_B \,\|\, r_\pi}{R_S + R_B \,\|\, r_\pi}\right) g_m}$$

$$R_C = \frac{-A_v}{\left(\frac{R_{B1} \,\|\, R_{B2} \,\|\, r_\pi}{R_S + R_{B1} \,\|\, R_{B2} \,\|\, r_\pi}\right) g_m} = \frac{50}{\left(\frac{39k\Omega \,\|\, 18k\Omega \,\|\, 1.9k\Omega}{50\Omega + 39k\Omega \,\|\, 18k\Omega \,\|\, 1.9k\Omega}\right) 0.0772\Omega^{-1}} = 667.3\Omega$$

For which you would still choose 680 Ω as the nearest "real" value.

• The only remaining task is to choose a "real" value for R_E, and again the nearest value is 1.8 kΩ.

• ***This gives the same result as we got by ignoring the input divider!!!***

R_C = 680 Ω R_E = 1.8 kΩ

R_{B1} = 39 kΩ R_{B2} = 18 kΩ

• We would still have had to adjust R_E to get the correct gain after simulating the circuit! HOWEVER (!), if R_S was greater than 50 Ω (for which the input divider gives a gain factor of 0.971), the input divider could have been much more significant. For example, if R_S were 1 kΩ, the gain gain factor from the input divider would be 0.622, which would mean that for an overall gain of -50, the CE stage itself would need a gain boost of $(0.622)^{-1}$, or 1.61 times.

• The moral of this story is that the way to tell whether or not the input divider is significant is to compare the magnitude of $R_{B1}||R_{B2}||r_\pi$ to R_S. If R_S is much smaller, it can often be ignored. If R_S is comparable, the attenuation from the input divider can be quite significant.

• Also note that r_π is a function of I_C, so adjusting I_C does have an effect on the input divider.

$$r_\pi = \frac{\beta}{g_m} = \frac{\beta v_T}{I_C}$$

Chapter 6: BJT FREQUENCY RESPONSE

... I have wasted a lot of time being fooled by a bad component - what do I do? I usually WIDLARIZE it, and it makes me feel a lot better. How do you WIDLARIZE something? You take it over to the anvil part of the vice, and you beat on it with a hammer, until it is all crunched down to tiny little pieces, so small that you don't even have to sweep it off the floor. It makes you feel better.
Bob Pease, Analog Guru, National Semiconductor

1: OBJECTIVES

• To begin estimating frequency responses of BJT amplifiers by learning about:

The junction capacitances of BJT's and their effects on frequency response.

The diffusion capacitance of BJT's and its effect on frequency response.

A frequency dependent and more complete Hybrid-π model.

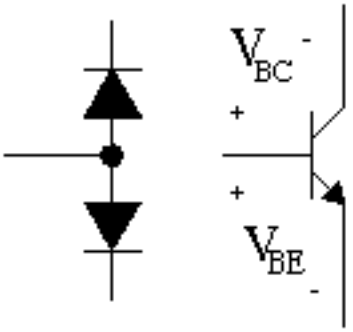
Estimating frequency response of a CE amplifier and seeing how the Miller Effect applies in that case.

READ S&S Section 7.5

2: JUNCTION CAPACITANCES OF BJT'S

• Both of the PN junctions in a BJT have junction capacitances which end up reducing the frequency response of the transistor.

• They are often referred to as C_{JE} and C_{JC} (or C_{BE} and C_{BC}, for the base-emitter and base-collector capacitances, respectively) as illustrated below:



NPN

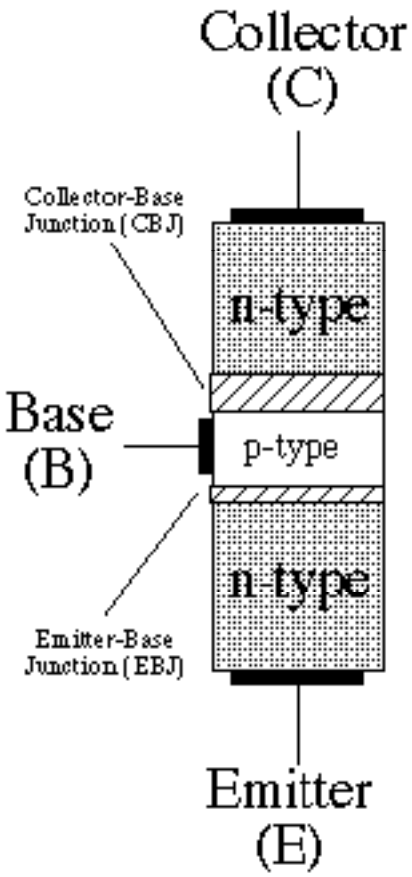
REMEMBER: for active mode (we are interested in AMPLIFIERS here!), the base-emitter junction is forward biased and the base-collector junction is reverse biased.

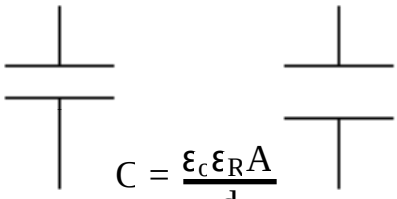
In normal (non-saturated) operation, C_{JC} is purely a depletion-region capacitance and is therefore dependent upon V_{BC} .....

Remember that for **REVERSE** bias, the depletion region **GROWS** in width!

-> this is like enlarging the distance between the plates of a parallel plate capacitor

-> **THE CAPACITANCE DECREASES WITH MORE NEGATIVE V_{BC}**





More negative V_{BC} = Smaller C_{JC}

$$C = \frac{\varepsilon_c \varepsilon_R A}{d}$$

This is analogous to a parallel-plate capacitor.

In normal (non-saturated) operation, C_{JE} is also a depletion-region capacitance and is therefore dependent upon V_{BE} .....

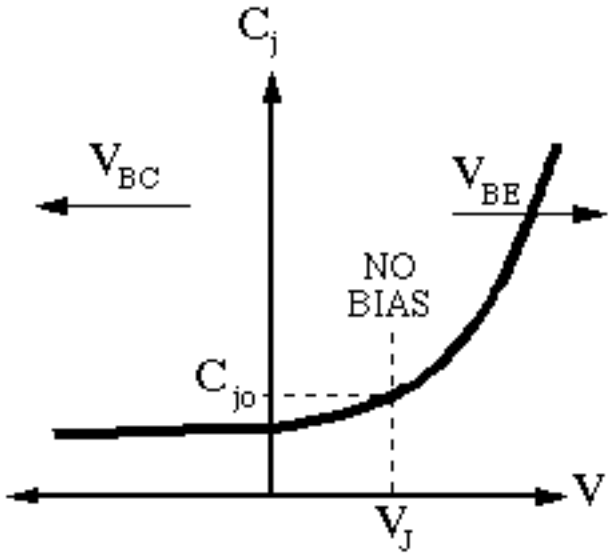
Remember that for **FORWARD** bias, the depletion region **SHRINKS** in width!

-> this is like shrinking the distance between the plates of a parallel plate capacitor

-> **THE CAPACITANCE INCREASES WITH MORE POSITIVE V_{BE}**

BIAS DEPENDENCE OF JUNCTION CAPACITANCES

• The junction capacitances are (nonlinearly) determined by the bias voltages as shown below.



• Actual estimation of the junction capacitances can be tricky. The equation shown below works fairly well for reverse-biased junctions.

$$C_j = \frac{C_{jo}}{\left(1 - \frac{V}{V_j}\right)^{m_j}}$$

where C_{jo} is the unbiased junction capacitance, V_j is the built-in potential of the junction (often called Ψ_o), and m_j is a constant between 0.3 and 0.5 depending on whether the junction is graded (0.3) or abrupt (0.5).

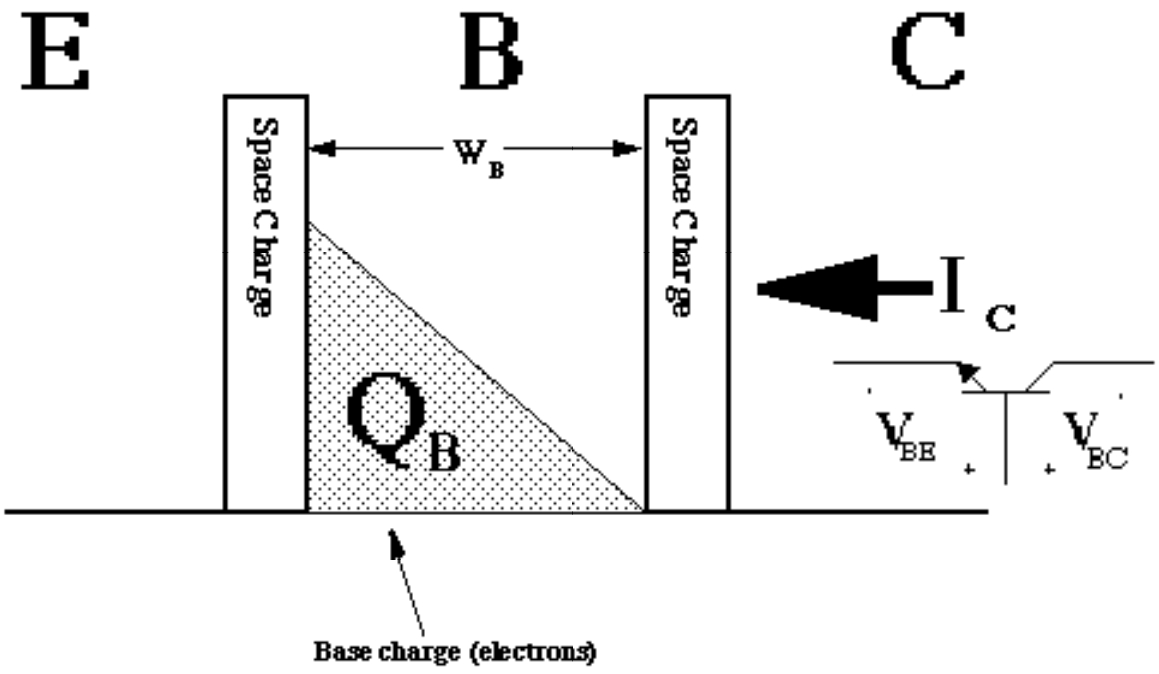
• For forward-biased junctions, the approximately generally used is that the capacitance is double that of the same junction under no bias.

3: DIFFUSION CAPACITANCE

• The diffusion capacitance appears between the BASE and EMITTER and is the result of the diffusion of minority carriers across the base.

• One can think about it as follows: if there is a certain number of carriers diffusing through the base, it takes a certain amount of time to adjust that number if the applied signal changes. Time delays in controlling currents are the hallmark of capacitances.

• For NPN transistors, electrons are the minority carriers in the base.



$$I_C = \frac{Q_B}{\tau_f} = \frac{\text{charge in base}}{\text{transit time for that charge to be swept through the base}}$$

$Q_B = I_C \tau_f$

$$C_d \equiv \frac{dQ_B}{dV_{BE}} = \tau_f \frac{dI_C}{dV_{BE}} = g_m \tau_f = g_m \frac{W_B^2}{2 D_B}$$

base width

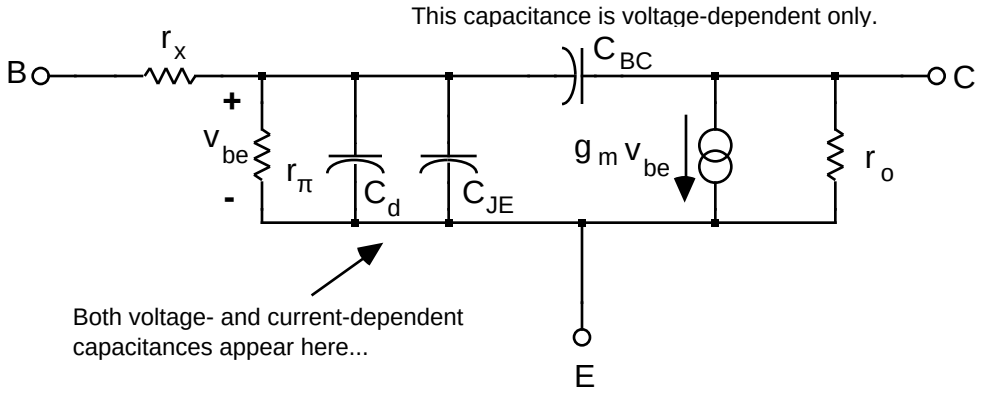
diffusivity of minority carriers in base

SUMMARY:

• AT LOW I_C -> C_{jc} and C_{je} DOMINATE

• AT HIGH I_C -> C_d DOMINATES

4: COMPLETE HYBRID-π MODEL

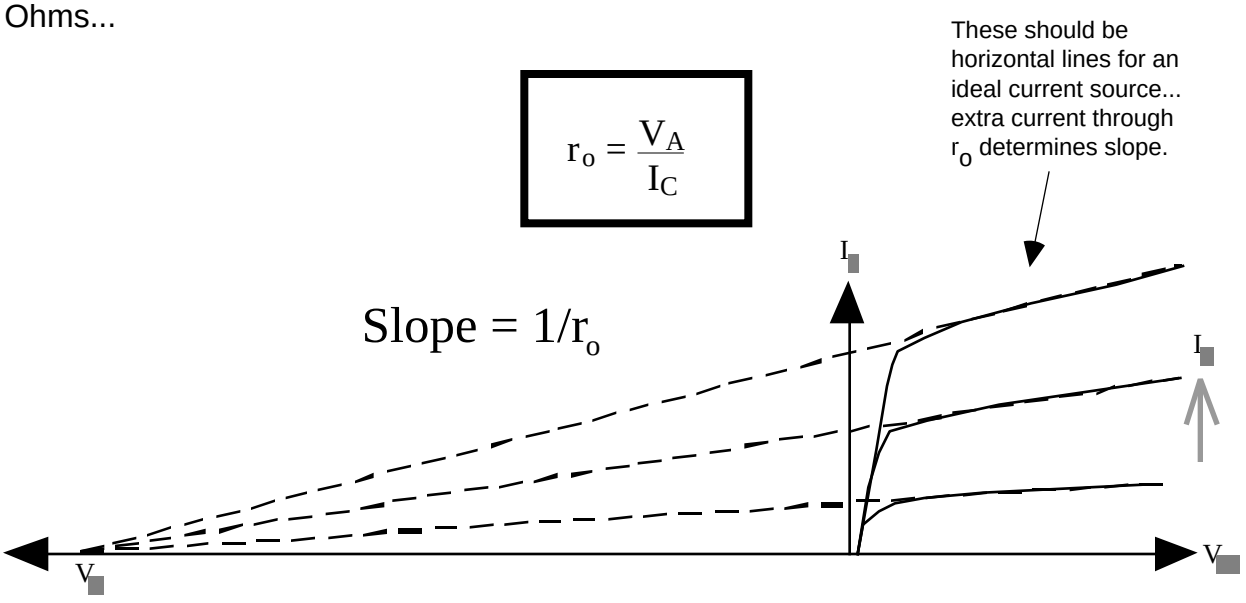


• r_x is the ohmic resistance of the base contact and is a **few tenths of ohms** normally.

• r_o is a resistance that models the slight effect of collector voltage on collector current in the active region of operation (the curves are not exactly flat!).

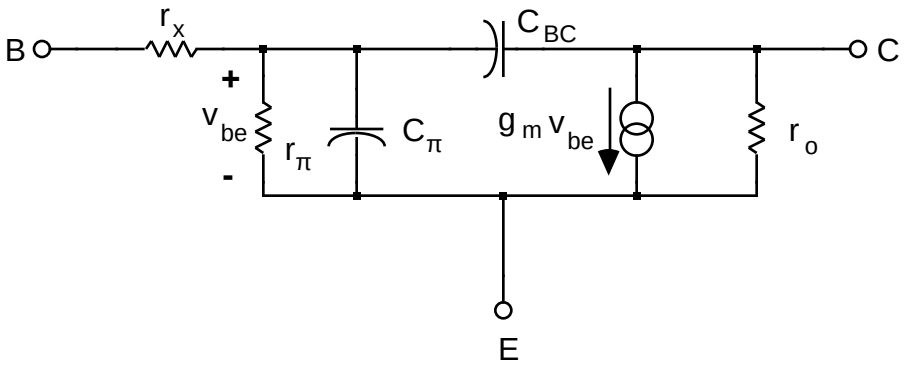
• r_o is inversely proportional to the DC bias current and is typically tens of thousands of Ohms...

$$r_o = \frac{V_A}{I_C}$$



• V_A is the Early voltage, which is discussed again below with respect to current sources.

• In practice, the two base-emitter capacitances are lumped together as c_π (or C_{BE} in SPICE).



• Typically r_x is in series with R_s (source resistance of the input signal generator) and r_o shunts R_C (the collector resistor, not shown above because it would be a part of the external circuit).

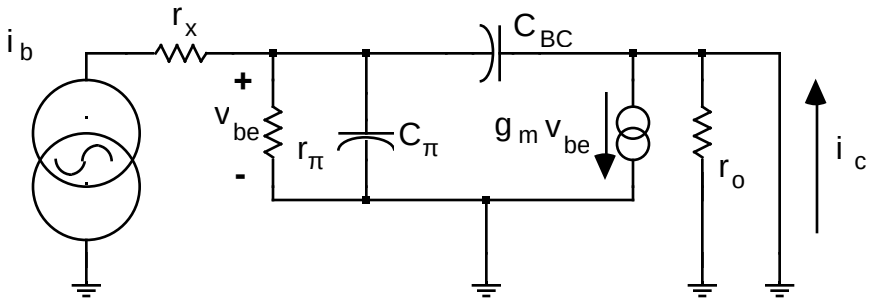
AVOID NOTATION CONFUSION!!!

$C_\pi \equiv C_d + C_{JE}(V_{BE})$ in SPICE, this is C_{BE}

$C_{JC}(V_{BE}) = C_{BC}$ in SPICE

5: GAIN (β) VERSUS FREQUENCY FOR BJT'S

• In order to understand the frequency response characteristics of the BJT, one needs to study the time constants of the BJT alone.



$$\beta(S) = \frac{i_c}{i_b} = \frac{g_m v_{be}}{i_b}$$

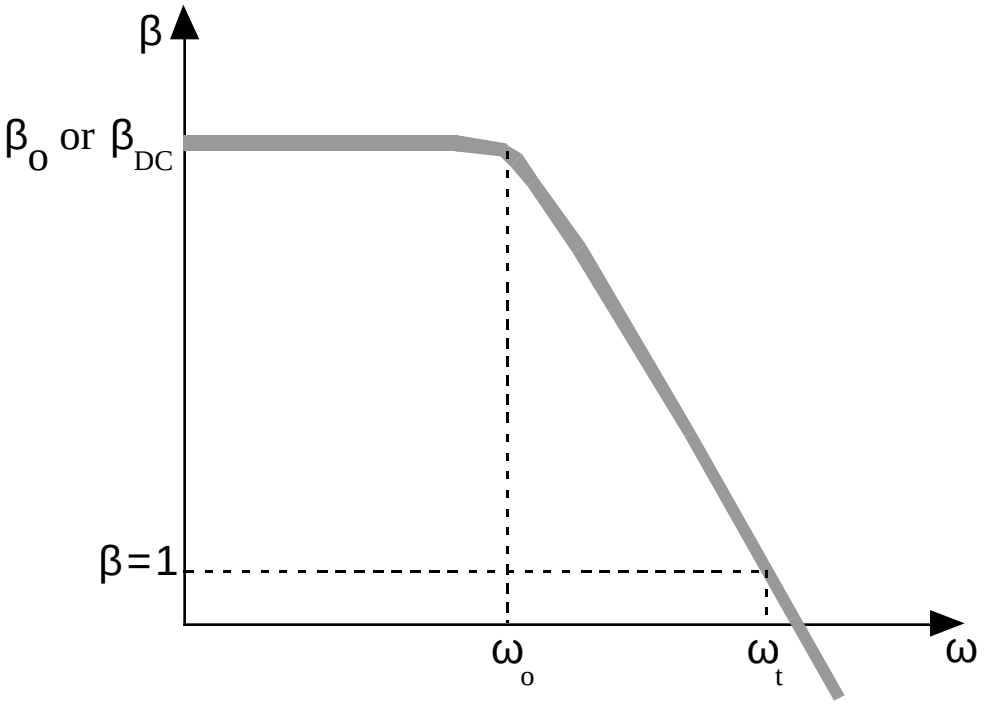
$$v_{be} = \frac{i_b}{\frac{1}{r_\pi} + S(C_\pi + C_{BC})}$$

$$\beta(S) = \frac{i_c}{i_b} = \frac{g_m}{\frac{1}{r_\pi} + S(C_\pi + C_{BC})} = \frac{g_m r_\pi}{1 + S r_\pi (C_\pi + C_{BC})} = \frac{\beta_o}{1 + S r_\pi (C_\pi + C_{BC})}$$

LOOKS LIKE A LOW-PASS FILTER!

$$\beta(S) = \frac{\beta_o}{1 + S\, r_\pi (C_\pi + C_{BC})} \qquad H(s) = \frac{K}{1 + \frac{s}{\omega_o}} \quad \text{OR} \quad \frac{K\omega_o}{\omega_o + s} = \frac{A}{\omega_o + s}$$

where $\omega_0 = 2\pi f_c = \frac{1}{\text{"RC"}} = \frac{1}{r_\pi (C_\pi + C_{BC})}$



A graphical representation of the decrease of β as frequency increases. β is 3 dB down at ω_o and β = 1 at ω_t. Note that Sedra and Smith refers to ω_o as ω_b.

• A key transistor parameter, ω_t , can now be derived. The unity-gain bandwidth, ω_t (or f_t in Hertz) is the frequency at which the **current gain (β)** of a transistor in **common-emitter** configuration, with its output short-circuited, **drops to unity**.

$$\beta(\omega_t) = 1 = \frac{\beta_o}{1 + S\, r_\pi (C_\pi + C_{BC})} = \frac{\beta_o}{1 + S \frac{\beta_o}{g_m}(C_\pi + C_{BC})}$$

solving,

$$1 + S \frac{\beta_o}{g_m}(C_\pi + C_{BC}) = \beta_o$$

This is independent of β_o !

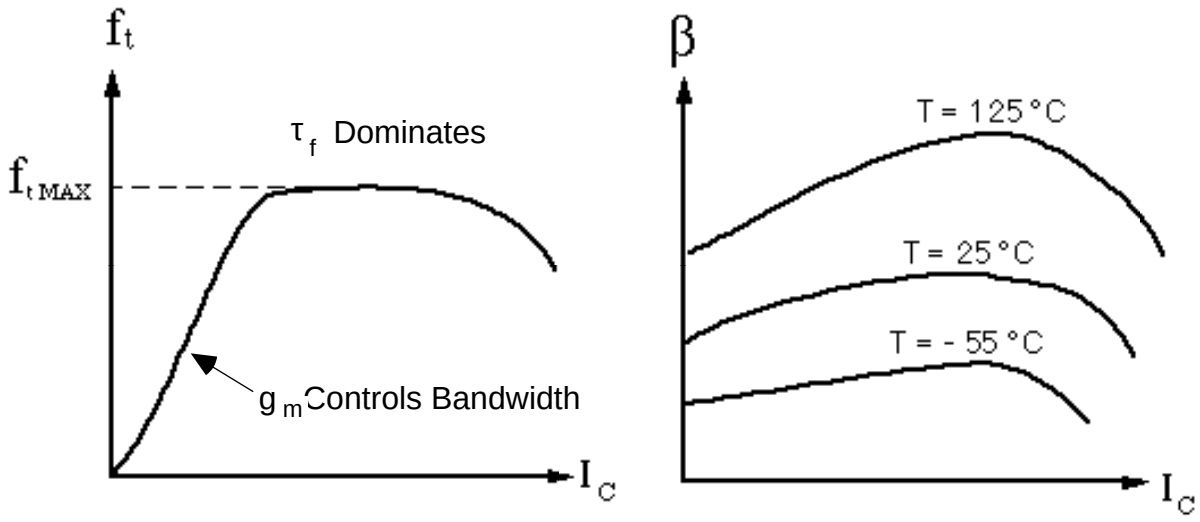
$$S = \omega_t = \frac{\beta_o - 1}{\frac{\beta_o}{g_m}(C_\pi + C_{BC})} \approx \frac{1}{\frac{1}{g_m}(C_\pi + C_{BC})}$$

• One can write this to show the contributions from different capacitance mechanisms,

$$2\pi f_t = \omega_t \approx \frac{1}{\frac{1}{g_m}(C_\pi + C_{BC})} = \frac{1}{\tau_f + \frac{C_{JE}}{g_m} + \frac{C_{BC}}{g_m}}$$

• One can increase I_c to increase bandwidth until τ_f dominates.

DESIGN NOTE: As you increase I_C, g_m goes up, so the last two terms decrease... The maximum possible f_t is then obtained, but then falls off if I_C continues to be increased because β_o falls off at high current anyway.



• By inspection of the above, it can be seen that that,

$$\omega_o = \frac{1}{r_\pi (C_\pi + C_{BC})} \qquad \text{(the 3dB frequency for } \beta)$$

TYPICAL VALUES FROM SPICE (EE122 PRELAB)

$$C_{BE} = 2.2 \text{ X } 10^{-11} \quad (C_d + C_{JE}(V_{BE}))$$

$$C_{BC} = 2.3 \text{ X } 10^{-12}$$

$$g_m = 1.43 \text{ X } 10^{-2}$$

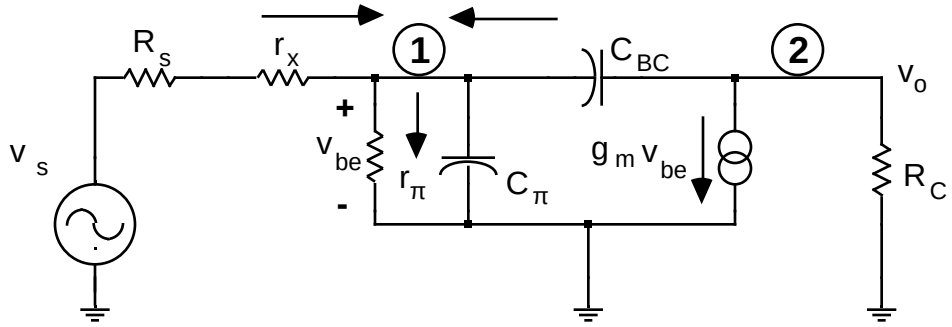
$$2\pi f_t = \omega_t \approx \frac{1}{\left(\frac{2.2 \text{ X } 10^{-11}}{1.43 \text{ X } 10^{-2}} + \frac{2.3 \text{ X } 10^{-12}}{1.43 \text{ X } 10^{-2}}\right)} = 5.88 \text{ X } 10^{8} \qquad \text{Radians}$$

$$f_t = 9.35 \text{ X } 10^{7} \qquad \text{Hertz} \qquad \text{->} \qquad 93.5 \text{ MHz}$$

THIS IS ALMOST EXACTLY WHAT SPICE PREDICTS (See Prelab)

6: COMMON-EMITTER CONFIGURATION AND MILLER CAPACITANCE

• The purpose of this effort is to examine the frequency response of the common emitter amplifier and see how the gain of the amplifier makes C_{BC} look really large thanks to the **Miller Effect**.



• For convenience, use $R_S' = R_S + r_x$

• START by looking at the circuit... It looks like any capacitance in the input circuit shorts out v_{be} as the frequency goes up...

• Summing currents at node (1)

$$\frac{v_s - v_{be}}{R_s'} + (v_o - v_{be})\, S\, C_{BC} = \left(\frac{1}{r_\pi} + S\, C_\pi\right) v_{be}$$

• Summing currents at node (2)

$$g_m v_{be} = -\frac{v_o}{R_C} - (v_o - v_{be})\, S\, C_{BC}$$

• Assuming that $v_o >> v_{be}$, can write,

$$v_o \approx -\frac{g_m v_{be}}{\left(\frac{1}{R_C} + S\, C_{BC}\right)}$$

• To further simplify, use the basic CE amplifier gain equation (assuming $1/R_c >> SC_{BC}$),

$$v_o \approx -\, g_m R_C v_{be}$$

• PLUG IT ALL TOGETHER....

The numerator is the DC gain.

$$A_v = \frac{v_o}{v_s} \approx \frac{-g_m R_C \left(\frac{r_\pi}{r_\pi + R_s'}\right)}{1 + S\left(r_\pi \,||\, R_s'\right)\left[C_\pi + \underbrace{C_{BC}\left(1 + g_m R_C\right)}_{C_{MILLER}}\right]}$$

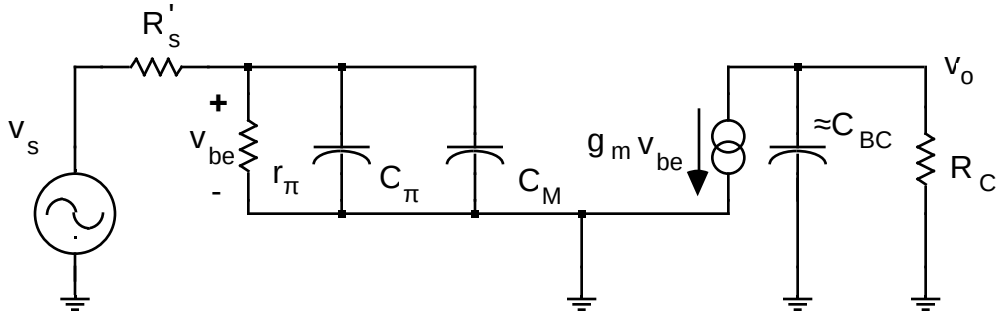
• Reminder of Miller's Theorem:

$Z_1 = \frac{Z_f}{1 - A}$ -> Miller impedance at the input of the amplifier

$Z_2 = Z_f \frac{-A}{1 - A}$ -> Miller impedance at the output of the amplifier

THE CIRCUIT REWRITTEN AS THE MILLER EQUIVALENT

• (Note that the output Miller equivalent of C_{BC} has been neglected because it is very small... also we are ASSUMING that the hybrid-π amplifier model's gain is not changed by C_{BC}... this is true for a model, but not always for a real amplifier and especially for larger capacitances, perhaps external to the transistors!)



$$C_M = C_{BC}\left(1 + g_m R_C\right)$$

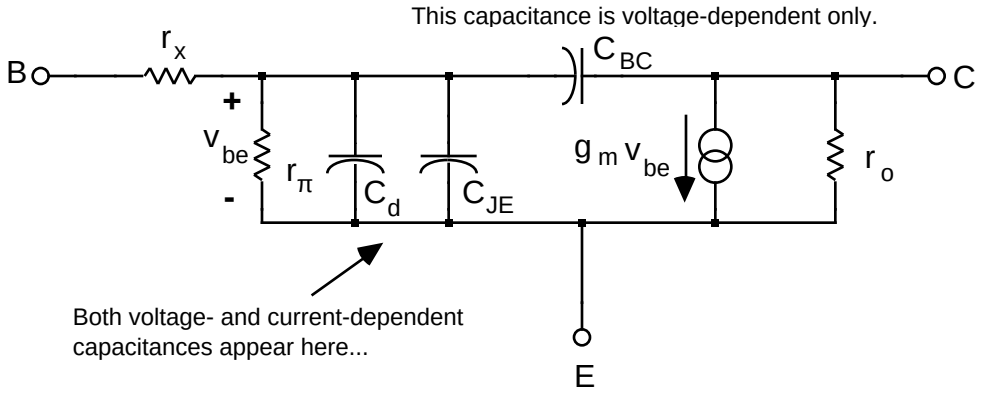
• So, in effect, a small input current makes $-g_m R_C$ times as much current flow into the output circuit... This makes C_{BC} seem much larger from the point of view of the input circuit!

• The **dominant pole** (more on this later) of CE amplifiers is determined by the input resistance and the input capacitances, C_π and C_M...

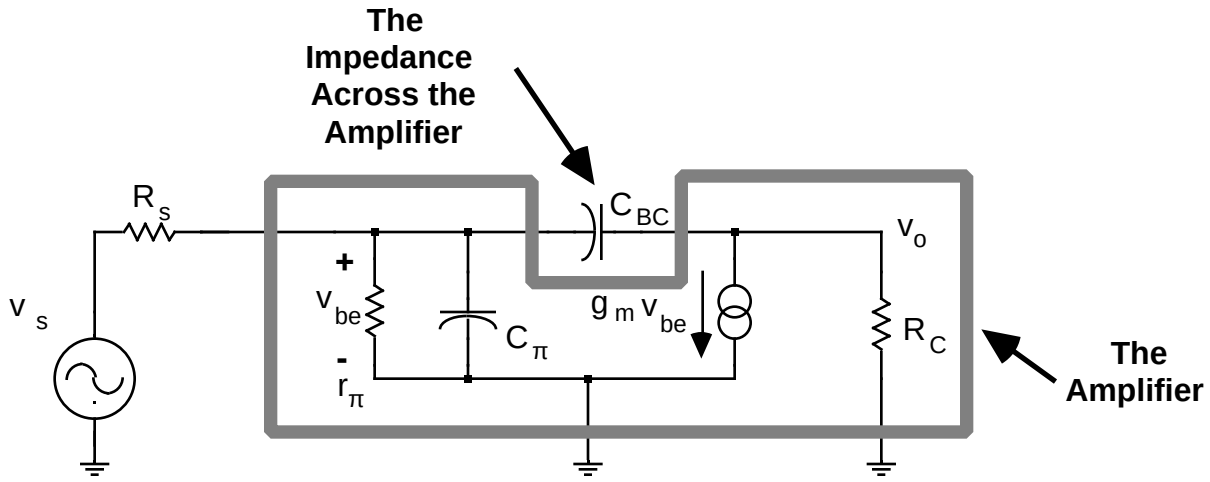
7: USING THE MILLER IDEA UP FRONT

• Here we are going to apply the Miller Effect idea **directly** to the complete hybrid-π model to simplify the circuit analysis. Remember that the idea is to convert an impedance across an amplifier into two separate (grounded) ones at the input and output.

• Here (again) is the "complete" hybrid-π model for a bipolar transistor:

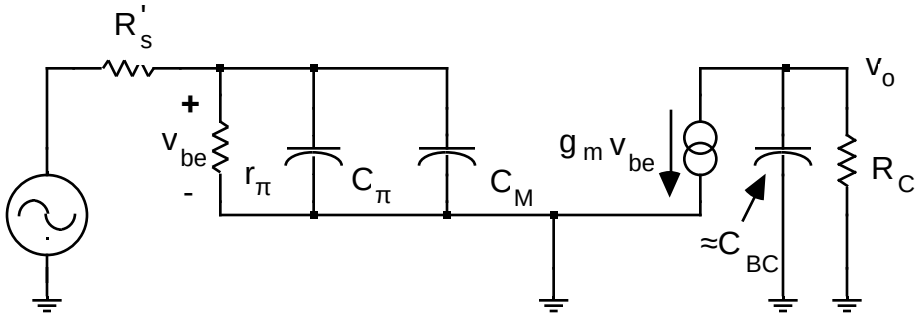


• Now throw in a collector resistance, R_C, to make it into a common emitter amplifier (no R_E)... also, let's **neglect** r_x and r_o!



• A very important point here is that the gain used in the Miller equation must be the gain seen by the component in question (here, that is C_{BC}). Thus, if there is an input voltage divider due to R_S, for example, one needs to compute the gain C_{BC} deals with, and the input divider does not affect that!

• The internal gain (relative to C_{BC}) is $-g_m R_c$ and one can re-write the circuit as the Miller equivalent, by multiplying C_{BC} by the (1 - gain) and putting it at the input, and multiplying C_{BC} by ≈1 and putting it at the output!



$$C_M = C_{BC}\left(1 + g_m R_C\right)$$

• Note that the maximum possible range of the scaled copy of C_{BC} at the output is between one and two times the value of C_{BC}, corresponding to infinite gain and a gain of one for the amplifier that C_{BC} straddles. This is discussed in detail below, and its "exact" value is given by,

$$C_{out} = C_{BC}\,\frac{1 + g_m\left(R_C \parallel R_L \parallel r_o\right)}{g_m\left(R_C \parallel R_L \parallel r_o\right)}$$

• One can **sometimes** ignore C_{out} at the output because if R_C is relatively low, the time constant due to a few picoFarads is not much... however, at high frequencies, it may start to matter!

• Also, if we are talking about a multi-stage amplifier, C_{out} now appears at the **INPUT** of the next stage... then it can be significant!

PLEASE REMEMBER THIS STUFF... WE WILL USE THIS TECHNIQUE OF TAKING THE MILLER EQUIVALENT OF C_{BC} MANY TIMES IN THE FUTURE!

Chapter 7: GENERAL AMPLIFIER FREQUENCY RESPONSE

If I tell you to neglect the effects of the junction capacitances, you'd better just do it, little man!
Arnold Schwarzenegger as Robo-Prof

1: OBJECTIVES

• To learn about:

The generalized frequency response of capacitor-coupled amplifiers.

Short-circuit and open-circuit time constants for approximating the response of amplifiers.

How coupling and bypass capacitors affect the (LOW) frequency response of amplifiers by studying a common emitter example.

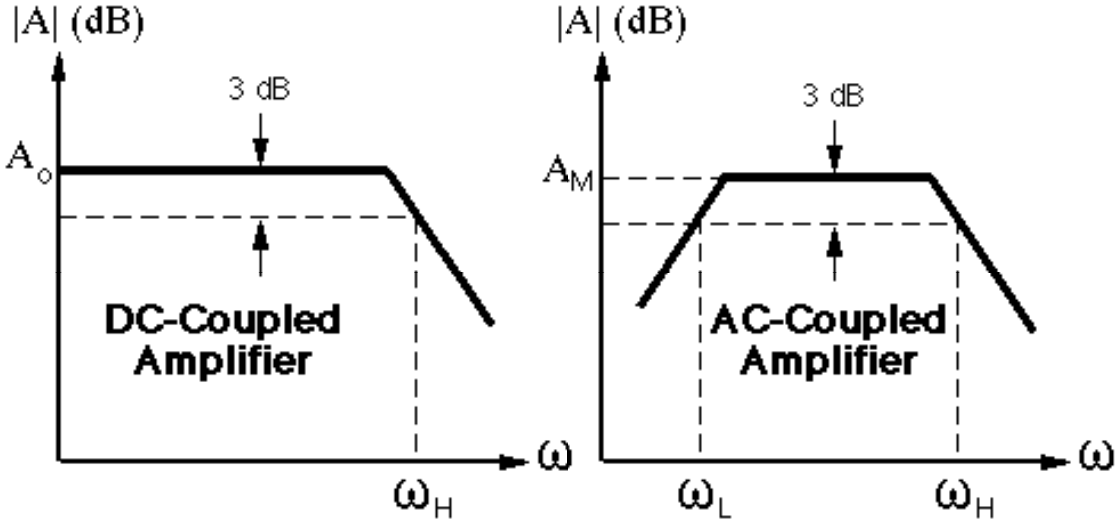
READ S&S Sections 7.2, 7.4 (don't worry that it's done with a FET!), and 7.6

REVIEW: How to make Bode Plots (S & S Section 7.1)

THE POINT OF ALL OF THIS: We want to know how to take a circuit and determine its frequency response.

An overall goal of this is to be able to analyze a circuit and then know how to DESIGN a circuit with the frequency response we need!

2: GENERALIZED CAPACITOR-COUPLED AMPLIFIER FREQUENCY RESPONSE



• The two plots above represent DC-coupled (left) and AC-coupled (right) amplifiers. The single transistor amplifiers generally need input and output coupling capacitors so that external DC voltages do not shift the bias point. Thus, these will have AC-coupled responses. Differential amplifiers (presented below) are DC-coupled.

• For the AC-coupled response, near ω_L and below, the amplifier's response acts like a **high-pass filter**.

• For both cases, near ω_H and above, the amplifier's response acts like a **low-pass filter**.

• The (hopefully) flat region in the middle is the "mid-band." We typically talk about the "mid-band gain" of an AC-coupled amplifier.

• It is important to note that one can look at the transfer function of an AC-coupled amplifier as the **product** of the high-pass, mid-band, and low-pass transfer functions,

$$A(S) = A_M F_L(S) F_H(S)$$

Reminder: The impedance of a capacitor is,

$$Z_C = \frac{1}{SC} \quad \text{or, for sinusoidal steady-state} = \frac{1}{2\pi fC}$$

Thus, they are open-circuits at DC and shorts at very high frequencies.

3: DOMINANT POLES

• Dominant poles are poles that dominate over the others in the transfer function so that the low- or high-frequency response of an amplifier can be approximated as a first-order high- or low-pass filter. (**REMEMBER** that op-amps are *DELIBERATELY* designed to have a single dominant pole -> this is so we will be able to predict their response and use it!).

DOMINANT LOW-FREQUENCY POLE

• If there is a dominant low-frequency pole (this is the one that acts like a **HIGH-PASS** filter), the low-frequency response can be approximated as,

$$F_L(S) \approx \frac{S}{S + \omega_{P1}}$$

• So, if the "full" low-frequency response is,

$$F_L(S) = \frac{(S + \omega_{Z1})(S + \omega_{Z2}) \bullet\bullet\bullet\bullet (S + \omega_{ZNL})}{(S + \omega_{P1})(S + \omega_{P2}) \bullet\bullet\bullet\bullet (S + \omega_{PNL})}$$

this means that ω_{P1} is at a much **HIGHER** frequency than the other poles so that it can DOMINATE...

• Note that the number of poles and zeros must be equal (at that point) if the function "flattens out" in the mid-band!

• If there is no dominant pole, you can make the following approximation,

$$\omega_L \approx \sqrt{\sum_{n=1}^{N} \omega_{Pn}^2 - 2 \sum_{n=1}^{N} \omega_{Zn}^2}$$

DOMINANT HIGH-FREQUENCY POLE

• If there is a dominant high-frequency pole (this is the one that acts like a **LOW-PASS** filter), the high-frequency response can be approximated as,

$$F_H(S) \approx \frac{1}{1 + \frac{S}{\omega_{P1}}}$$

• So, if the “full” high-frequency response is,

$$F_H(S) = \frac{\left(1 + \frac{S}{\omega_{Z1}}\right)\left(1 + \frac{S}{\omega_{Z2}}\right) \bullet\bullet\bullet\bullet \left(1 + \frac{S}{\omega_{ZNH}}\right)}{\left(1 + \frac{S}{\omega_{P1}}\right)\left(1 + \frac{S}{\omega_{P2}}\right) \bullet\bullet\bullet\bullet \left(1 + \frac{S}{\omega_{PNH}}\right)}$$

this means that ω_{P1} is at a much **LOWER** frequency than the other poles so that it can DOMINATE...

Note that the number of poles and zeros must be equal (at that point) if the function “flattens out” in the mid-band!

• If there is no dominant pole, you can make the following approximation,

$$\omega_H \approx \frac{1}{\sqrt{\sum_{n=1}^{N} \frac{1}{\omega_{Pn}^2} - 2\sum_{n=1}^{N} \frac{1}{\omega_{Zn}^2}}}$$

4: SHORT-CIRCUIT AND OPEN-CIRCUIT TIME CONSTANT METHODS FOR APPROXIMATING THE RESPONSE OF AMPLIFIERS

• This is a very useful method for approximating upper and lower cut-off frequencies, assuming that there is a dominant pole (it works pretty well if there isn’t too!).

• Depending on which of the two methods you use, for each capacitor in the circuit, you replace the capacitors in the circuit, except for the one you are looking at, with either shorts or opens.

• Two key rules apply to both methods:

1) DISABLE all independent sources...
voltage sources -> SHORT CIRCUIT
current sources -> OPEN CIRCUIT

2) DO NOT remove or “disable” dependent sources!

4.1 OPEN-CIRCUIT TIME CONSTANTS FOR UPPER CUT-OFF FREQUENCY APPROXIMATION

• All you have to do is step through the process of calculating a “local” RC time-constant for each capacitor in the circuit.

For each capacitor you set all other capacitances (other than the one you are looking at) to zero (i.e. they become OPEN CIRCUITS as if they have not yet had any effect on the amplifier's roll-off) and determine the resistance, R_{io}, seen by C_i (the capacitor you are working with).

• Repeat this process for each capacitor.

• The upper cut-off frequency is then approximately given by,

$$\omega_H \approx \frac{1}{\left[\sum_i C_i R_{io}\right]}$$

This approach can tell you which of the capacitances in a circuit is most significant in determining the high-frequency response!

4.2 SHORT-CIRCUIT TIME CONSTANTS FOR LOWER CUT-OFF FREQUENCY APPROXIMATION

• Again, all you have to do is step through the process of calculating a “local” RC time-constant for each capacitor in the circuit.

For each capacitor you set all other capacitances (other than the one you are looking at) to INFINITY (i.e. they become SHORT CIRCUITS as if they have already become low enough impedance to neglect) and determine the resistance, R_{iS}, seen by C_i (the capacitor you are working with).

• Repeat this process for each capacitor.

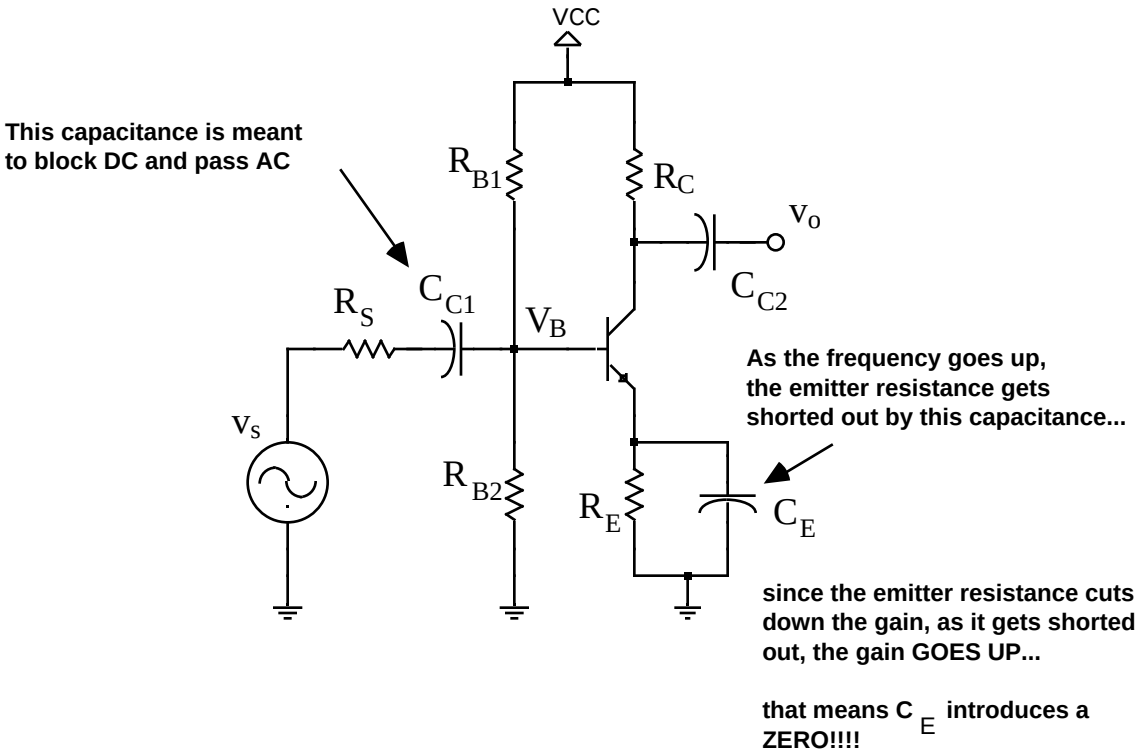
• The lower cut-off frequency is then approximately given by,

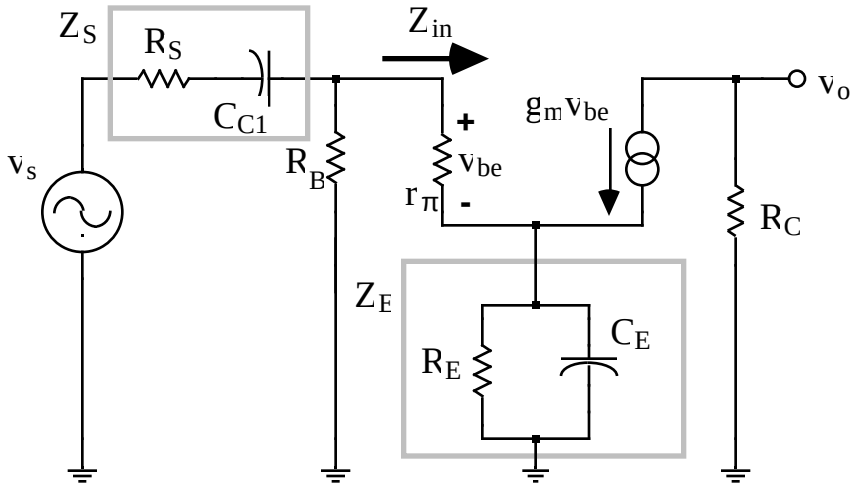
$$\omega_L \approx \sum_i \frac{1}{C_i R_{iS}}$$

This approach can tell you which of the capacitances in a circuit is most significant in determining the low-frequency response!

5: FREQUENCY RESPONSE OF THE CE AMPLIFIER

• This circuit should be familiar from previous lectures and from EE122! The point of this section is to GRIND through the derivation of its frequency response "the hard way," and then **compare** to the response obtained using the open- and short-circuit time constant approximations....





$$Z_S = \frac{1 + S\,R_S C_{C1}}{S\,C_{C1}} \qquad Z_E = \frac{R_E}{1 + S\,R_E C_E}$$

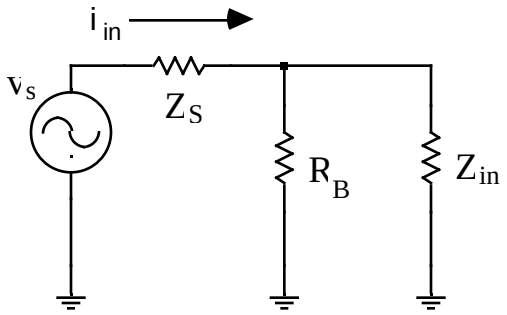
• **REMEMBER** from the case where R_E is not bypassed, that one can take R_E into account when looking from the base using the rule that lets you multiply its resistance by (1 + β). HERE IS THAT POINT AGAIN, GENERALIZED FOR IMPEDANCES!

> One can "transform" an impedance from the emitter or base side of the base emitter circuit to the opposite side just as one would for just a resistance. An impedance in the emitter circuit will appear as being (β+1) times ***larger*** when viewed from the base terminal. Similarly, an impedance in the base circuit will appear as being (β+1) times ***smaller*** when viewed from the emitter terminal.

Using this, we can write,

$$Z_{in} = r_\pi + (\beta + 1) Z_E$$ (here R_{in} is for the transistor, NOT the entire amplifier!)

5.1 LOW FREQUENCY RESPONSE



$$i_{in} = \frac{v_s}{\left(1 + \frac{Z_{in}}{R_B}\right) Z_S + Z_{in}}$$

FROM HERE ON, ASSUME R_B = INFINITY TO SIMPLIFY THINGS!

$$i_{in} = \frac{v_s}{Z_s + Z_{in}} = \frac{v_s}{Z_s + r_\pi + (\beta+1) Z_E} = \frac{v_s}{\frac{1 + SR_SC_{C1}}{SC_{C1}} + r_\pi + (\beta+1)\frac{R_E}{1 + SR_EC_E}}$$

• Grinding through the math and regrouping terms,

$$\frac{i_{in}}{v_s} = \frac{(S\,C_{C1})(1 + S\,R_EC_E)}{1 + S\left\{C_{C1}\left[R_S + r_\pi + (\beta+1)\,R_E\right] + R_EC_E\right\} + S^2\left(R_SC_{C1}R_EC_E + r_\pi C_{C1}R_EC_E\right)}$$

• A nice, second-order transfer function for the input conductance....

• Looking at the numerator first, there is a ZERO at $\omega = 0$ (because of C_{C1}), and ZEROs are what we are typically expecting for low frequency analysis.

• There is a ZERO at $\omega = \frac{1}{R_EC_E}$

$$\frac{v_o}{v_s} = \beta\, R_C\, i_{in}$$

$$\frac{v_o}{v_s} = \frac{(\beta R_CC_{C1})(R_EC_E)\,S\left(S + \frac{1}{R_EC_E}\right)}{1 + S\left\{C_{C1}\left[R_S + r_\pi + (\beta+1)\,R_E\right] + R_EC_E\right\} + S^2\left(R_SC_{C1}R_EC_E + r_\pi C_{C1}R_EC_E\right)}$$

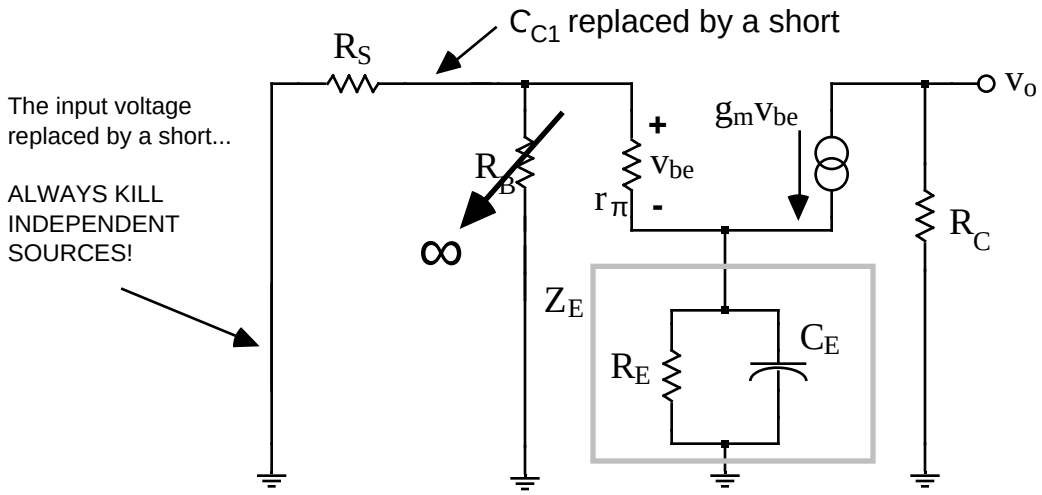
$$\frac{v_o}{v_s} = \left(\frac{\beta R_C}{R_S + r_\pi}\right) \frac{S\left(S + \dfrac{1}{R_E C_E}\right)}{S^2 + S\left[\dfrac{1}{C_E\left(R_E \parallel \dfrac{R_S + r_\pi}{(\beta+1)}\right)} + \dfrac{1}{C_{C1}\left(R_S + r_\pi\right)}\right] + \dfrac{1}{R_E C_E C_{C1}\left(R_S + r_\pi\right)}}$$

• This is of the form,

$$F_L(S) = \frac{S(S + \omega_{Z1})}{(S + \omega_{P1})(S + \omega_{P2})} = \frac{S(S + \omega_{Z1})}{S^2 + S(\omega_{P1} + \omega_{P2}) + \omega_{P1}\omega_{P2}}$$

• This was a lot of work!!!! Compare and see if the short- and open-circuit time constant methods agree. Begin by computing ω_L using the short-circuit time constant approximation.

• For C_E, (REMEMBER that we assumed **R_B = INFINITY** for simplicity) short C_{C1},



• **Note** that R_C is effectively "invisible" to C_E, since it cannot effect v_{be} (**that might not be true with feedback!**) and hence the current flowing in R_E and C_E... you can prove it to yourself by applying a test current... intuitively, R_C can't be "seen" through the current source.

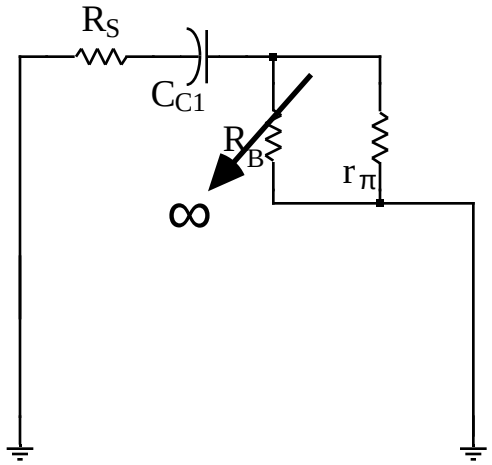
• Taking into account (ß+1) scaling,

$$R_{CES} = R_E \parallel \frac{R_S + r_\pi}{\beta + 1} = R_E \parallel \left(r_e + \frac{R_S}{\beta + 1}\right)$$

• If $R_B \neq \infty$ (or is not large enough to assume that), one obtains,

$$R_{CES} = R_E \parallel \frac{(R_S \parallel R_B) + r_\pi}{\beta + 1} = R_E \parallel \left(r_e + \frac{(R_S \parallel R_B)}{\beta + 1} \right)$$

• For C_{C1} short out C_E,



$$R_{C1S} = R_S + r_\pi$$

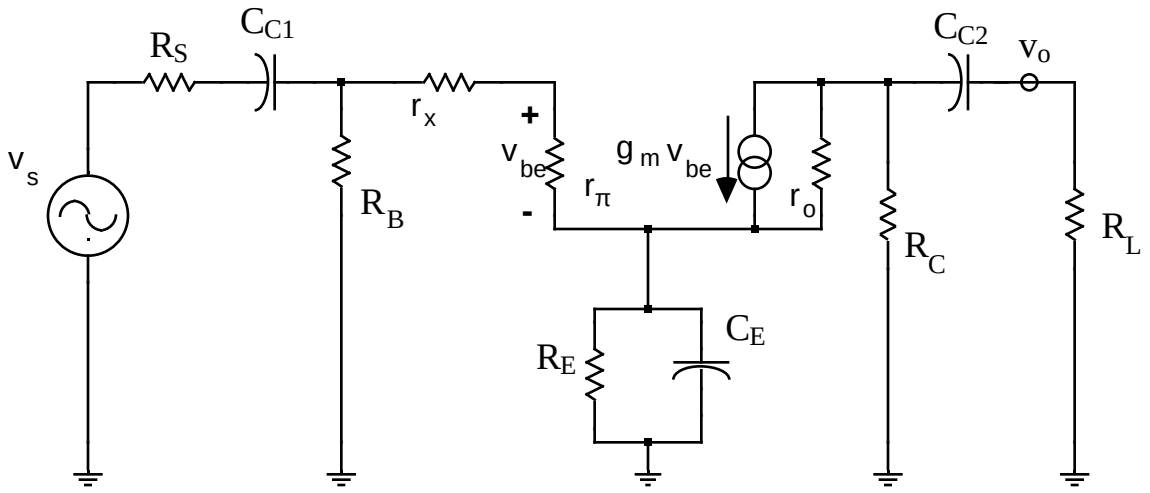
• These two RC time constants are the same as those found analytically....

$$\frac{v_o}{v_s} = \left(\frac{\beta R_C}{R_S + r_\pi} \right) \frac{S\left(S + \frac{1}{R_E C_E}\right)}{S^2 + S\left[\frac{1}{C_E\left(R_E \parallel \frac{R_S + r_\pi}{(\beta + 1)}\right)} + \frac{1}{C_{C1}(R_S + r_\pi)} \right] + \frac{1}{R_E C_E C_{C1}(R_S + r_\pi)}}$$

$$R_{ES} = R_E \parallel \frac{R_S + r_\pi}{\beta + 1}$$

$$R_{C1S} = R_S + r_\pi$$

• If you do not assume $R_B = \infty$, include r_x and r_o, consider the load resistance R_L, and consider an output coupling capacitor C_{C2} between the g_m generator and $R_C \parallel R_L$, you get the following results (S & S p. 529),



Using the method of short-circuit time constants,

$$\omega_L \approx \sum_i \frac{1}{C_i R_{iS}}$$

$$\omega_L \approx \frac{1}{C_{C1}R_{C1S}} + \frac{1}{C_E R_{ES}} + \frac{1}{C_{C2}R_{C2}}$$

Where,

$$R_{C1S} = R_S + \left[R_B \parallel \left(r_x + r_\pi\right)\right] \qquad \textbf{(INPUT)}$$

(remember that the other caps are shorts!)

$$R_{ES} = R_E \parallel \left[\frac{r_x + r_\pi + \left(R_B \parallel R_S\right)}{\beta + 1}\right] \qquad \textbf{(EMITTER)}$$

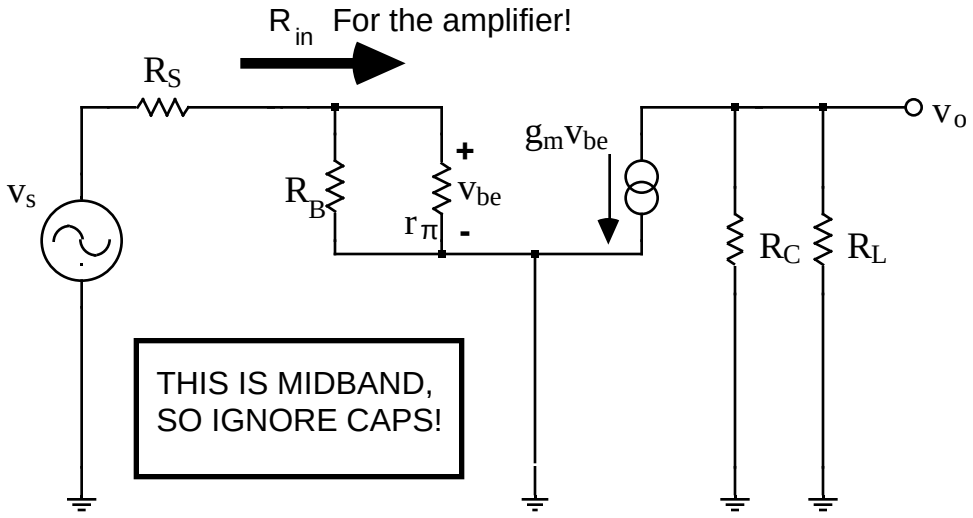
(remember about dividing by [β + 1] to reflect the input circuit impedances to the emitter circuit!)

$$R_{C2S} = R_L + \left(R_C \parallel r_o\right) \qquad \textbf{(OUTPUT)}$$

The zero introduced by C_E is at $\omega_{ZE} = \frac{1}{C_E R_E}$

5.2 MID-FREQUENCY RESPONSE

• Here assume all coupling and bypass capacitors are shorted (i.e. C_{C1}, C_{C2}, and C_E). You do not really need to worry too much yet (at midband frequencies) about the parasitic capacitances inside the BJT. They matter at higher frequencies.



$$R_{in} = R_B \,||\, r_\pi$$

$$R_B = R_{B1} \,||\, R_{B2}$$

$$v_{be} = \left(\frac{R_{in}}{R_s + R_{in}}\right) v_s$$

$$v_o = -\, g_m\, v_{be} \left(R_C \,||\, R_L\right)$$

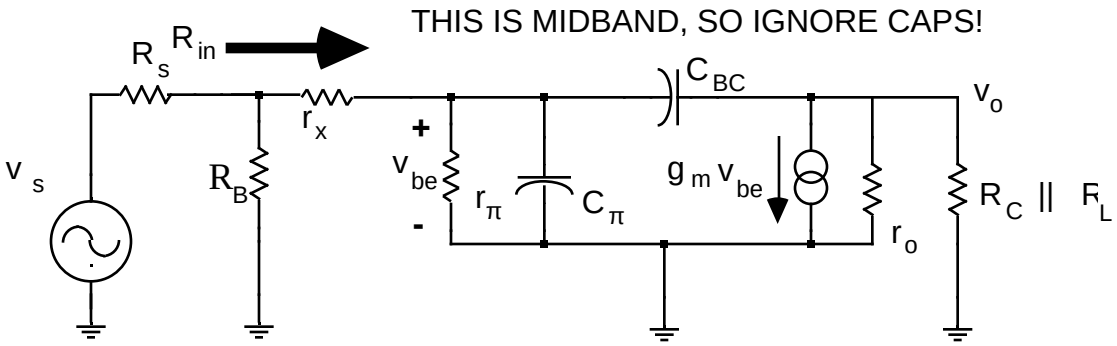
$$A_v = \frac{v_o}{v_s} = \left(\frac{R_{in}}{R_s + R_{in}}\right) (-\, g_m\,) \left(R_C \,||\, R_L\right)$$

• **NOTE** that r_o is not shown above... to take it into account, it can be placed in parallel with R_C and R_L.

• **Remember that the overall gain is,**

$$A_V(S) = \mathrm{LFgain}(S) \times \mathrm{MBgain} \times \mathrm{HFgain}(S)$$

• WHAT IF WE ADD IN THE "DETAILS" (i.e. CONSIDER R_L, r_o and r_x)?



$$R_{in} = R_B \parallel (r_x + r_\pi)$$

$$R_B = R_{B1} \parallel R_{B2}$$

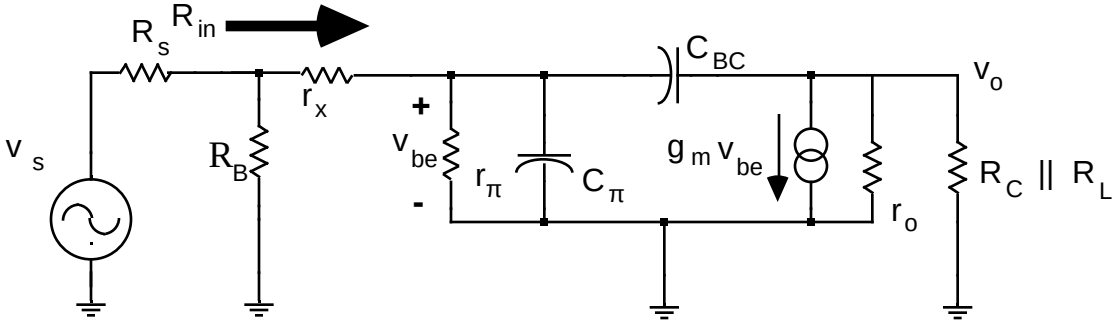
$$v_{be} = \left(\frac{R_{in}}{R_s + R_{in}}\right)\left(\frac{r_\pi}{r_\pi + r_x}\right) v_s$$

$$v_o = -\, g_m\, v_{be}\left(R_C \parallel R_L \parallel r_o\right)$$

$$A_v = \frac{v_o}{v_s} = \left(\frac{R_{in}}{R_S + R_{in}}\right)\left(\frac{r_\pi}{r_x + r_\pi}\right)\left(-g_m\right)\left(R_C \parallel R_L \parallel r_o\right)$$

5.3 HIGH-FREQUENCY RESPONSE

• From here up in frequency, we will start to worry about the **details of what's inside the BJT**! Now it matters, so use the "full" Hybrid-π model...



• **Note** that in some cases, you may need to compute the required capacitances for the model using,

$$2\pi f_t = \frac{1}{\frac{C_\pi}{g_m} + \frac{C_{BC}}{g_m}} \qquad \text{(remember that } C_\pi = C_d + C_{JE}\text{)}$$

• First, it is necessary to calculate the **Miller** capacitance to obtain a value for the total input capacitance,

$$C_{in} = C_\pi + C_M = C_\pi + C_{BC}\left(1 - A_{VQ}\right) \qquad \text{NOTE that S \& S use } C_\mu \text{ instead of } C_{BC}$$

• This is based on A_{VQ} which we will define as the **voltage gain between the two transistor terminals straddled by C_{BC}.... (IN OTHER WORDS, NOT SIMPLY THE OVERALL GAIN OF THE AMP!)** For this amplifier, you know that you want,

$$A_{VQ} = \frac{v_o}{v_{be}} = \left(-g_m\right)\left(R_C \parallel R_L \parallel r_o\right)$$

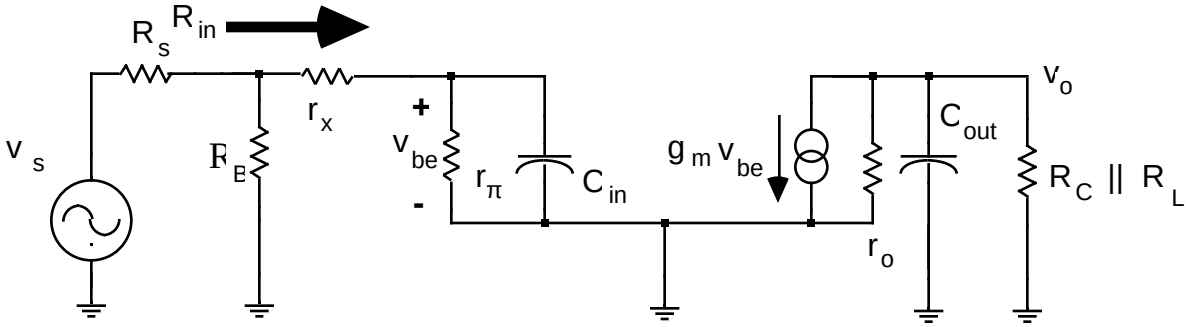
• Thus, we find that the Miller capacitance is given by,

$$\boxed{C_M = C_{BC}\left[1 + g_m\left(R_C \parallel R_L \parallel r_o\right)\right]}$$

• The output capacitance, C_{out} is given by,

$$C_{out} = C_{BC}\,\frac{1 + g_m\left(R_C \parallel R_L \parallel r_o\right)}{g_m\left(R_C \parallel R_L \parallel r_o\right)}$$

• This reduces the input circuit to a **first-order low-pass filter** (unless C_{out} is significant), so we do not need to use the method of open-circuit time constants.



The upper 3 dB frequency of the input circuit is often given by,

$$\omega_H = \frac{1}{R' C_{in}}$$

Where,

$$R' = r_\pi \,||\, \left(r_x + R_B \,||\, R_S\right)$$

and

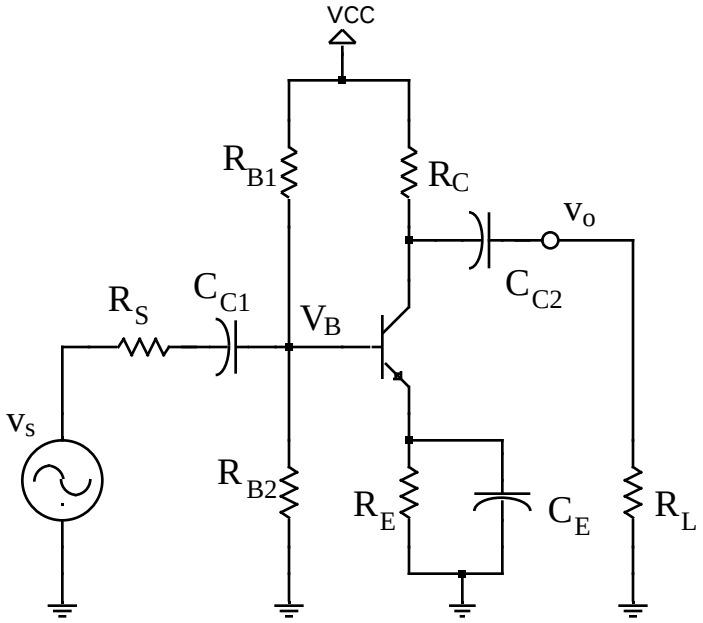
$$C_{in} = C_\pi + C_M = C_\pi + C_{BC}\left[1 + g_m\left(R_C \,||\, R_L \,||\, r_o\right)\right]$$

• NOTE that in some cases, the upper cut-off frequency may be determined by the output circuit (i.e. C_μ and $r_o||R_C||R_L$). This is very important to check!

• A more general approach would be to use Miller and then open-circuit time constants,

$$\omega_H \approx \frac{1}{\left[\sum_i C_i R_{io}\right]} = \frac{1}{C_{in} R' + C_{out} R_{out}} = \frac{1}{C_{in}\left(r_\pi \,||\left[r_x + R_B \,||\, R_S\right]\right) + C_{out}\left(r_o \,||\, R_C \,||\, R_L\right)}$$

6: EXAMPLE FREQUENCY RESPONSE ANALYSIS



• Following the example on page 530, Sedra & Smith (Exercises 7.14 - 7.19)

R_S = 4 kΩ R_{B1} = 8 kΩ R_{B2} = 4 kΩ R_E = 3.3 kΩ R_C = 6 kΩ R_L = 4 kΩ
V_{CC} = 12 V $I_E \approx$ 1 mA β_o = 100 C_π = 13.9 pF C_μ = 2 pF r_o = 100 kΩ
r_x = 50 Ω

6.1 MID-BAND GAIN CALCULATION

• NEGLECTING R_L, r_o and r_x ...

$$A_V = \frac{v_o}{v_s} = \left(\frac{R_B \,||\, r_\pi}{R_S + R_B \,||\, r_\pi}\right)(-g_m)\left(R_C \,||\, R_L\right)$$

$$g_m = \frac{I_C}{v_T} \approx \frac{1\ \text{mA}}{25.9\ \text{mV}} = 0.039\ \Omega^{-1}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{0.039\ \Omega^{-1}} = 2.56\ \text{k}\Omega$$

$$R_B = R_{B1} \,||\, R_{B2} = 8\ \text{k}\Omega \,||\, 4\ \text{k}\Omega = 2.67\ \text{k}\Omega$$

$$R_{in} = R_B \,||\, r_\pi = 2.67\ \text{k}\Omega \,||\, 2.56\ \text{k}\Omega = 1.31\ \text{k}\Omega$$

$$A_V = \frac{v_o}{v_s} = \left(\frac{2.67\ k\Omega\ ||2.56\ k\Omega}{4\ k\Omega + 2.67\ k\Omega\ ||2.56\ k\Omega}\right)\left(-0.039\ \Omega^{-1}\right)(6\ k\Omega\ ||\ 4\ k\Omega)$$

$$A_V = (0.247)\left(-0.039\ \Omega^{-1}\right)(2.4\ k\Omega) = -23.1$$

• Do the analysis again with "the details,"

$$R_{in} = R_B\ ||\ (r_x + r_\pi) = 2.67\ k\Omega\ ||\ (50\ \Omega + 2.56\ k\Omega) = 1.32\ k\Omega$$

$$A_v = \frac{v_o}{v_s} = \left(\frac{R_B\ ||\ (r_x + r_\pi)}{R_S + R_B\ ||\ (r_x + r_\pi)}\right)\left(\frac{r_\pi}{r_x + r_\pi}\right)(-g_m)(R_C\ ||\ R_L\ ||\ r_o)$$

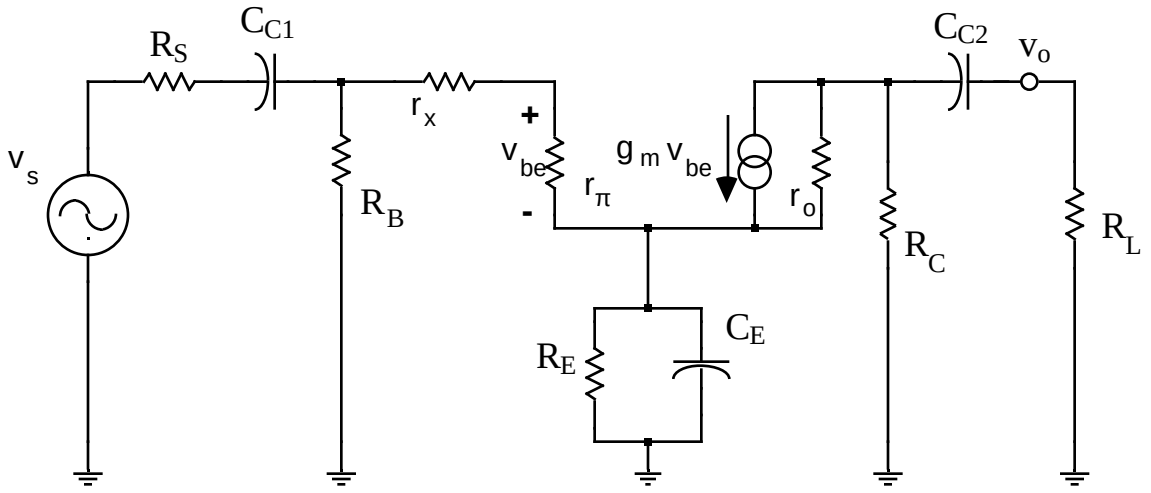
$$= \left(\frac{1.32\ k\Omega}{4\ k\Omega + 1.32\ k\Omega}\right)\left(\frac{2.56\ k\Omega}{50\ \Omega + 2.56\ k\Omega}\right)(-0.037)(6\ k\Omega\ ||4\ k\Omega\ ||100\ k\Omega)$$

$$= (0.248)(0.981)\left(-0.039\ \Omega^{-1}\right)(2.34\ k\Omega) = -22.2$$

$$A_v = (0.248)\,(0.981)\,(-0.039)\,(2.34\ K\Omega) = -22.2\ V/V$$

• There is not much difference between the two gain values. The key to this type of analysis is to know when you can approximate and when you cannot.

6.2 LOW-FREQUENCY RESPONSE



• Given: $C_{C1} = C_{C2} = 1\ \mu F$ and $C_E = 10\ \mu F$ (not infinity, so must use SC time constants), use,

$$\omega_L \approx \frac{1}{C_{C1}R_{C1S}} + \frac{1}{C_E R_{ES}} + \frac{1}{C_{C2}R_{C2}}$$

Where,

$$R_{C1S} = R_S + \left[R_B \parallel \left(r_x + r_\pi\right)\right] = 4\ k\Omega + \left[2.67\ k\Omega \parallel \left(50\ \Omega + 2.56\ k\Omega\right)\right] = 5.32\ k\Omega$$

$$R_{ES} = R_E \parallel \left[\frac{r_x + r_\pi + \left(R_B \parallel R_S\right)}{\beta + 1}\right]$$

$$R_{ES} = 3.3\ k\Omega \parallel \left[\frac{50\ \Omega + 2.56\ k\Omega + \left(2.67\ k\Omega \parallel 4\ k\Omega\right)}{100 + 1}\right] = 41.2\ \Omega$$

$$R_{C2S} = R_L + \left(R_C \parallel r_o\right) = 4\ k\Omega + \left(6\ k\Omega \parallel 100\ k\Omega\right) = 9.66\ k\Omega$$

What components control the low cut off frequency?

Can you "design" it?

$$\omega_L \approx \frac{1}{C_{C1}R_{C1S}} + \frac{1}{C_E R_{ES}} + \frac{1}{C_{C2}R_{C2}}$$

$$\omega_L \approx \frac{1}{\left(1\ X\ 10^{-6}\right)\left(5.32\ K\right)} + \frac{1}{\left(10\ X\ 10^{-6}\right)\left(41.2\right)} + \frac{1}{\left(1\ X\ 10^{-6}\right)\left(9.66\ K\right)}$$

$\omega_L \approx 188.0 + 2{,}427 + 103.5 = 2{,}719$ Radians -> $f_L \approx 432.7$ Hz

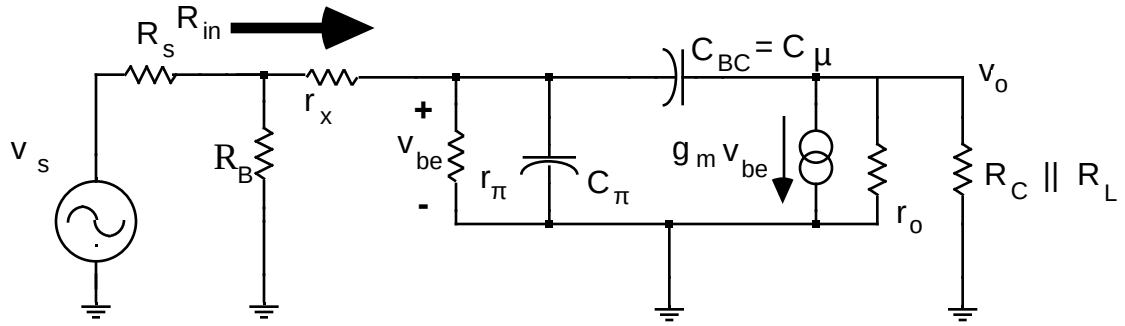
And, the frequency of the zero caused by the bypass capacitor on the emitter resistor being finite in size is,

$$\omega_{ZE} = \frac{1}{C_E R_E} = \frac{1}{10\ \text{X}\ 10^{-6}\ 3.3\ \text{K}\Omega} \quad \text{->} \quad f_{ZE} = 4.8\ \text{Hz}$$

(note that it is not R_E' above, but R_E)

6.3 HIGH-FREQUENCY RESPONSE

• From here up in frequency, we will start to worry about the details of what's inside the BJT. Now those junction capacitances matter, so one needs to use the "full" Hybrid-π model.



• Note (for homework) that you may need compute the required capacitances for the model using,

$$2\pi f_t = \frac{1}{\frac{C_\pi}{g_m} + \frac{C_{BC}}{g_m}}$$

• In the present example, we are given the values,

$C_\pi = 13.9$ pF $\qquad C_\mu = C_{BC} = 2$ pF

• First, we calculate the Miller capacitance to obtain a value for the total input capacitance (this gives the dominant high-frequency pole...)

$$C_M = C_{BC}\left[1 + g_m\left(R_C \parallel R_L \parallel r_o\right)\right] \quad \textbf{(note dependence on load resistance!)}$$

$$C_M = 2\ \text{X}\ 10^{-12}\left[1 + \left(0.039\right)\left(6\ \text{K}\Omega \parallel 4\ \text{K}\Omega \parallel 100\ \text{K}\Omega\right)\right] = 184.8\ \text{pF}$$

• From this, we see that the total input capacitance is,

$$C_{in} = C_{\pi} + C_M = 198.7 \text{ pF}$$

• The upper 3 dB frequency of the input circuit is given by,

$$\omega_H = \frac{1}{R' C_{in}}$$

Where,

$$R' = r_{\pi} \,||\, (r_x + R_B \,||\, R_s) = 2.56 \text{ K}\Omega \,||\, (50\ \Omega + 2.67 \text{ K}\Omega \,||\, 4 \text{ K}\Omega\ ) = 1.00 \text{ K}\Omega$$

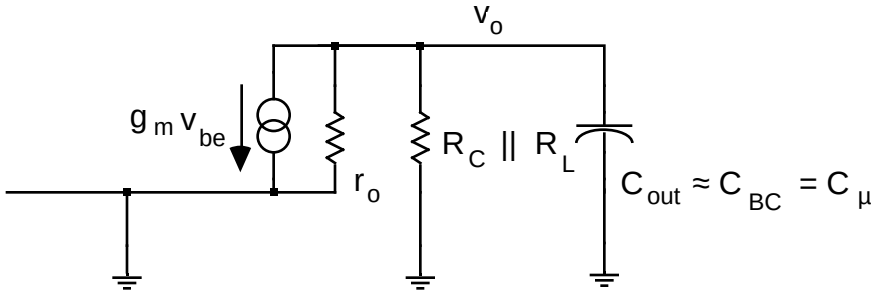
• So, $\omega_H = \dfrac{1}{(1.00 \text{ K})(199 \text{ X } 10^{-12})} = 5.025 \text{ X } 10^6 \text{ Radians}$ -> $f_H = 800 \text{ KHz}$

• Remember that there is a scaled "copy" of C_{BC} connected from the output to ground due to the Miller Effect.... what would that time constant be?

$$C_{out} = C_{BC} \frac{1 + g_m (R_C \,||\, R_L \,||\, r_o)}{g_m (R_C \,||\, R_L \,||\, r_o)} = (2 \text{ X } 10^{-12}) \frac{1 + (0.039\ \Omega^{-1})(6 \text{ k}\Omega \,||\, 4 \text{ k}\Omega \,||\, 100 \text{ k}\Omega)}{(0.039\ \Omega^{-1})(6 \text{ k}\Omega \,||\, 4 \text{ k}\Omega \,||\, 100 \text{ k}\Omega)}$$

$$C_{out} = (2 \text{ X } 10^{-12})(1.01) = 2.02 \text{ X } 10^{-12}$$

• Note that the value of C_{out}, for reasonably small gains like those typical in single-transistor amplifiers, is nearly the same as C_{BC}.



$$R'_{out} = r_o \,||\, R_L \,||\, R_C = 100\text{K}\Omega \,||\, 4\text{K}\Omega \,||\, 6\text{K}\Omega = 2.34 \text{ K}\Omega$$

$$\omega_{out} = \frac{1}{R'_{out} C_{BC}} = \frac{1}{2.34 \text{ K}\Omega \ 2 \text{ pF}} = 214 \text{ X } 10^6 \text{ Radians} = 34 \text{ MHz}$$

• So, ***in this case*** , it is pretty clear that the input time constant dominates at 800 kHz!

• One can always use the "full" approximation:

$$\omega_H \approx \frac{1}{\left[\sum_i C_i R_{io}\right]} = \frac{1}{C_{in}R' + C_{out}R_{out}} = \frac{1}{C_{in}\left(r_\pi \| \left[r_x + R_B \| R_S\right]\right) + C_{out}\left(r_o \| R_C \| R_L\right)}$$

DO NOT ASSUME THAT YOU CAN IGNORE THE OUTPUT TIME CONSTANT! (i.e. make sure the time constant caused by the Miller copy of C_{BC} at the output is not a significant one!)

•A "full" analysis for the upper cut-off frequency could also be done using the open-circuit time constants method, but would not provide additional information in this case due to the relative simplicity of the circuit.

Chapter 8: THE COMMON BASE AMPLIFIER

22% of fast food employees in the U.S.
admit to doing, "slow, sloppy work on purpose."
Harper's Index

1: OBJECTIVES

• To learn about:

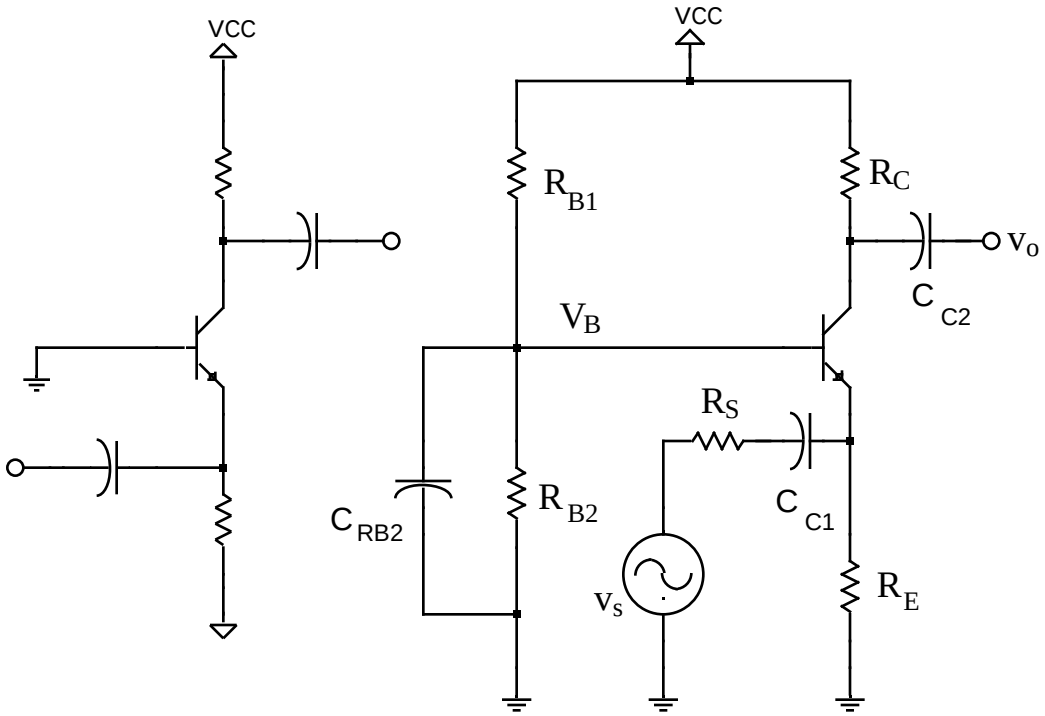
Common base amplifier analysis.

Common base amplifier frequency response.

The basics of a two-transistor amplifier, the *cascode* amplifier, based on the CE and CB stages in combination.

READ S&S Section 7.7

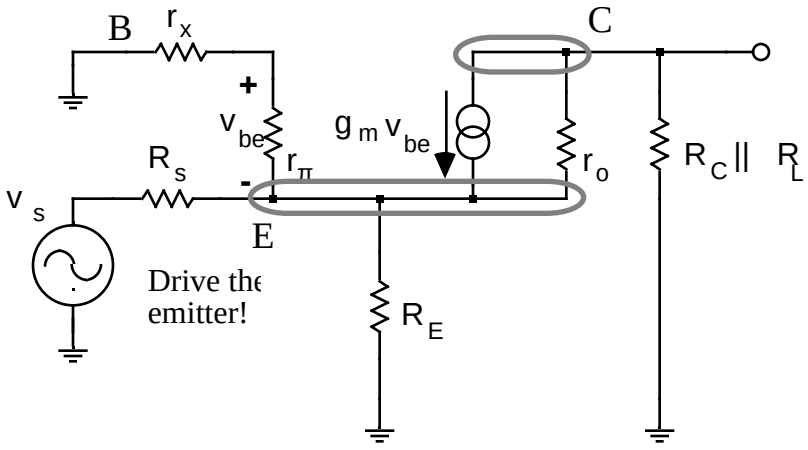
2: THE COMMON BASE CIRCUIT



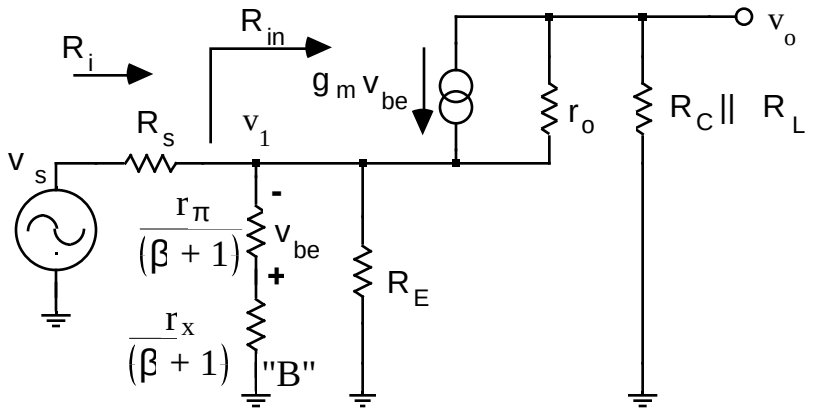
• Note that the base can either be tied **directly to ground** or (more common) **it can be biased using the "classic" scheme discussed for the common-emitter amplifier** with one difference -> one of the bias resistors should be bypassed so that the parallel combination of R_{B1} and R_{B2} has "zero" impedance for AC signals!

3: MID-BAND GAIN CALCULATIONS

• First, make a small-signal equivalent of the circuit on the above right (more general):



• Transform the base resistances to the emitter circuit by dividing by (β + 1),



then compute v_{be} as a function of v_s, starting with an intermediate voltage, v_1,

$$v_1 = \frac{\left[R_E \parallel \frac{(r_\pi + r_x)}{(\beta + 1)}\right]}{\left[R_E \parallel \frac{(r_\pi + r_x)}{(\beta + 1)}\right] + R_S} v_s$$

v_1 is a fraction of v_s given by voltage division

$$v_{be} = - \frac{\frac{r_\pi}{(\beta + 1)}}{\frac{r_\pi}{(\beta + 1)} + \frac{r_x}{(\beta + 1)}} v_1 = - \frac{r_\pi}{r_\pi + r_x} v_1$$

similarly, v_{be} is a fraction of v_1

combining these gives,

$$v_{be} = - \frac{r_\pi}{r_\pi + r_x} \frac{\left[R_E \parallel \frac{(r_\pi + r_x)}{(\beta + 1)}\right]}{\left[R_E \parallel \frac{(r_\pi + r_x)}{(\beta + 1)}\right] + R_S} v_s$$

• If we assume that $r_x \approx 0$ (not an unreasonable assumption, since typical values are less than 50 Ω, but certainly r_x is << r_π),

$$v_{be} = - \frac{\left[R_E \parallel \frac{r_\pi}{(\beta + 1)}\right]}{\left[R_E \parallel \frac{r_\pi}{(\beta + 1)}\right] + R_S} v_s = - \frac{\left[R_E \parallel r_e\right]}{\left[R_E \parallel r_e\right] + R_S} v_s$$

• This further simplifies if R_s = 0 (i.e. the CB amplifier is driven by a very low output impedance stage)...

$$v_{be} = - \ v_s$$

• Now for the output stage, assuming r_o is "approximately grounded" or, simply very large compared to R_C and R_L,

$$v_o \approx -g_m v_{be}\left(R_C \parallel R_L \parallel r_o\right) \approx -g_m v_{be}\left(R_C \parallel\parallel R_L\right)$$

which gives,

$$A_V \equiv \frac{v_o}{v_s} = \frac{\left(R_E \parallel r_e\right)}{\left(R_E \parallel r_e\right) + R_S} g_m \left(R_C \parallel\parallel R_L\right)$$

and for $R_E >> r_e$, this simplifies to,

NON-INVERTING!

$$\boxed{A_V = \frac{r_e}{r_e + R_S} g_m \left(R_C \parallel\parallel R_L\right)}$$

• If r_o were considered in parallel with R_C and R_L, it would clearly reduce gain.

• Again **neglecting r_o** and r_x, the input resistance is seen to be,

$$\boxed{R_i = R_S + R_E \parallel\parallel r_e \approx R_S + r_e}$$

• **NOTE** that we typically do **NOT** include R_S into our expression for R_{IN} because it is **not** a part of the common-base amplifier itself!.... don't let this confuse you!

• Remember that,

$$r_e = \frac{r_\pi}{1+\beta} \approx \frac{r_\pi}{\beta} = \frac{1}{g_m} = \frac{V_T}{I_C}$$

• This means **you can control r_e** and hence the input resistance via I_C.

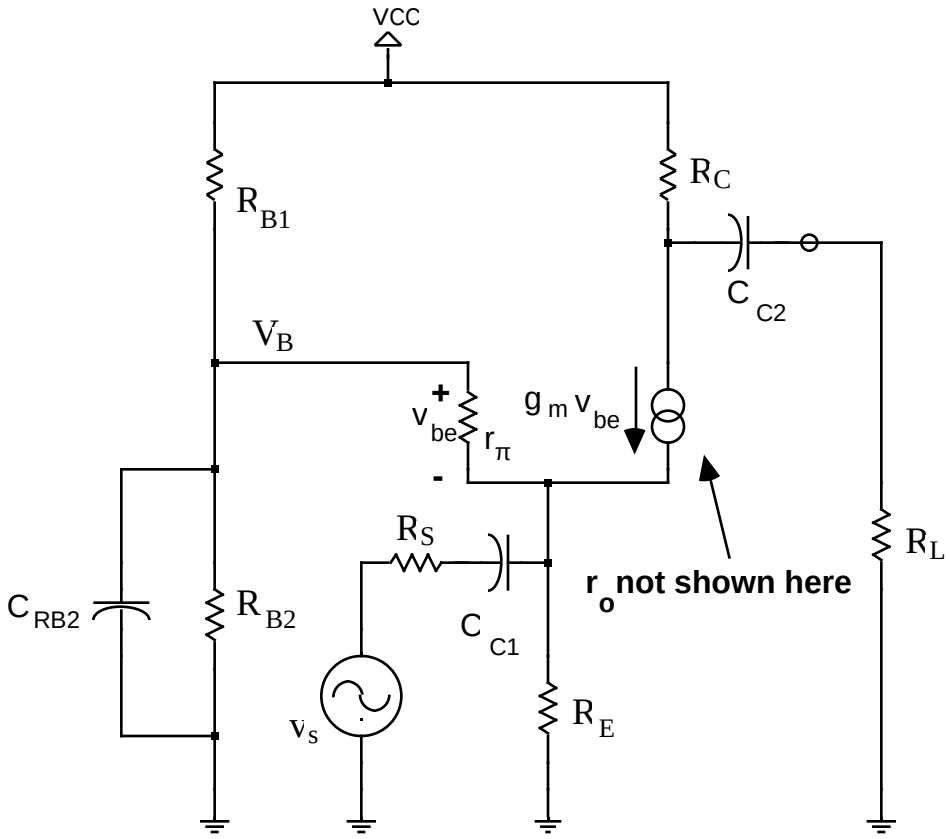
$$R_{IN} = R_E \parallel r_e \approx r_e$$

• To determine the output resistance, we set $v_s = 0$ and remove R_L (since it is not part of the amplifier itself) and see that,

$$R_o = R_C$$

• One can include r_o in parallel with R_C for added accuracy, if necessary... if r_o is comparable to R_C this can be quite significant and reduce gain as well.

4: LOW-FREQUENCY RESPONSE



• Here the coupling and bypass capacitors matter!

• Using the method of **short-circuit time constants** (the one for **low** frequencies),

$$\omega_L \approx \frac{1}{C_{RB2}R_{RB2}} + \frac{1}{C_{C1}R_{C1}} + \frac{1}{C_{C2}R_{C2}}$$

where,

$$R_{RB2} = R_{B2} \,||R_{B1}|| \left[r_\pi + (\beta + 1)\left(R_E \,||\, R_S\right)\right]$$

$$R_{C1} = R_S + R_E \,||r_e$$

$$R_{C2} = R_C + R_L$$

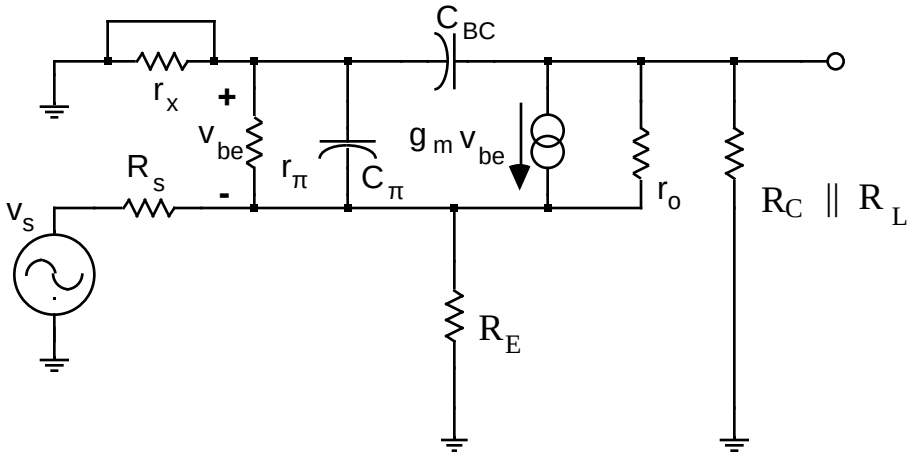
• Hopefully it is clear that if you **literally** ground the base, you don't need to consider R_{RB2}...

• **NOTE:** If you take into account r_o in parallel with the current source, you get a new time constant for C_{C2},

$$R_{C2} = R_C \,||\left(r_o + R_E \,||R_S \,||\, r_e\right) + R_L$$

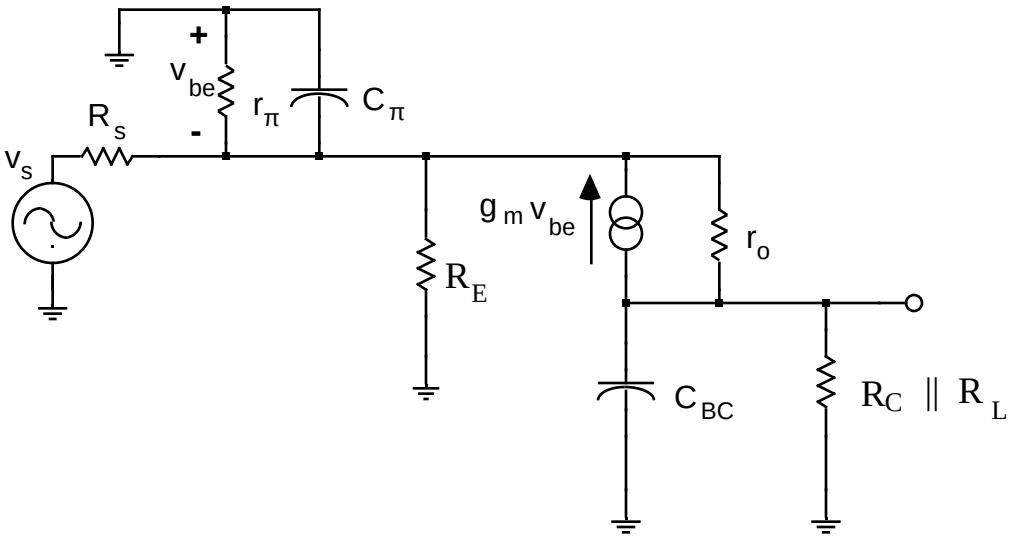
but since r_o is generally >> r_e, this doesn't change things much.

5: HIGH-FREQUENCY RESPONSE

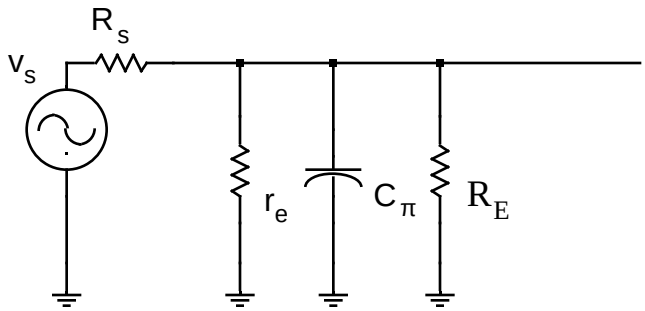


• Assuming r_x = 0, it is immediately clear the one terminal of C_{BC} is grounded... This means there is no Miller multiplication of its capacitance!

• The circuit is more intuitive if it is re-drawn knowing this (r_x no longer shown),



• We can see that the input circuit (after transforming r_π into r_e in the emitter circuit) looks like this:



• NOTE: **We don't scale C_π by (ß + 1)** because the extra current flowing due to the current source is already taken into account in transforming r_π into r_e (if we scaled C_π as well, the resulting pole would be "corrected" *twice* and therefore be wrong!).

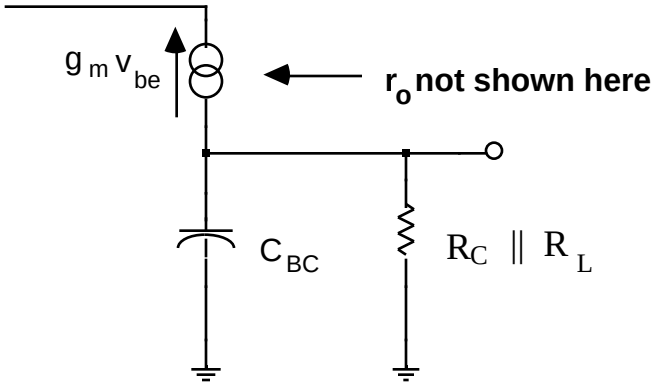
• In other words, the extra emitter current that we model in r_e is "real" as opposed to the capacitor current, which is "imaginary." Therefore, the extra current is fully modeled by r_e without modifying C_π.

• Still another way of looking at it is to consider that the capacitor current is determined by the voltage across it, v_{be}, which is the same, no matter which way you look (base or emitter). For r_π and r_e, the current is a function of which terminal you look into because at the emitter, you see the extra current from the source.

• Now we can **determine the input pole frequency** by setting the signal source to zero...

$$\omega_{P1} = \frac{1}{C_\pi\left(r_e \,\|\, R_E \,\|\, R_S\right)}$$

• Similarly, the **output stage's pole frequency can be determined** (neglecting r_o),



$$\omega_{P2} = \frac{1}{C_{BC}\left(R_C \,||R_L\right)}$$

• Since r_e is small, ω_{P1} will be a very high frequency. Since C_{BC} is small, ω_{P2} will also be a very high frequency.

• The high frequency response is (neglecting r_o),

$$\omega_H \approx \frac{1}{\sum_i C_i R_{io}} = \frac{1}{C_\pi\left(r_e \,||\, R_E \,||\, R_S\right) + C_{BC}\left(R_C \,||\, R_L\right)}$$

• For the CE amplifier we had derived (neglecting the output pole at $C_{BC}(r_o||R_C||R_L)$),

$$\omega_H \approx \frac{1}{R' C_{in}} = \frac{1}{r_\pi \,||\left(r_x + R_B \,||\, R_S\right)\left(C_\pi + C_{BC}\left[1 + g_m\left(R_C \,||\, R_L \,||\, r_o\right)\right]\right)}$$

assuming r_x is very small and r_o is very large, this simplifies to,

$$\omega_H = \frac{1}{R' C_{in}} = \frac{1}{\left(r_\pi \,||\, R_B \,||\, R_s\right)\left(C_\pi + C_{BC} + C_{BC}\, g_m \left(R_C \,||\, R_L\right)\right)}$$

• Take our previous example and compare...

R_S = 4 KΩ R_{B1} = 8 KΩ R_{B2} = 4 KΩ R_E = 3.3 KΩ R_C = 6 KΩ R_L = 4 KΩ
V_{CC} = 12 V $I_E \approx$ 1 mA β_o = 100 C_π = 13.9 pF C_μ = 2 pF r_o = 100 KΩ
r_x = 50 Ω

$$g_m = \frac{I_C}{V_T} \approx \frac{1\text{ mA}}{25.9\text{ mV}} = 0.039\ \Omega^{-1} \qquad r_\pi = \frac{\beta}{g_m} = \frac{100}{0.039\ \Omega^{-1}} = 2.56\ \text{K}\Omega$$

$$r_e = \frac{1}{g_m} = 25.6\ \Omega$$

$$f_{HCE} = 800\ \text{KHz}$$

$$f_{HCB} = 30.9\ \text{MHz}$$

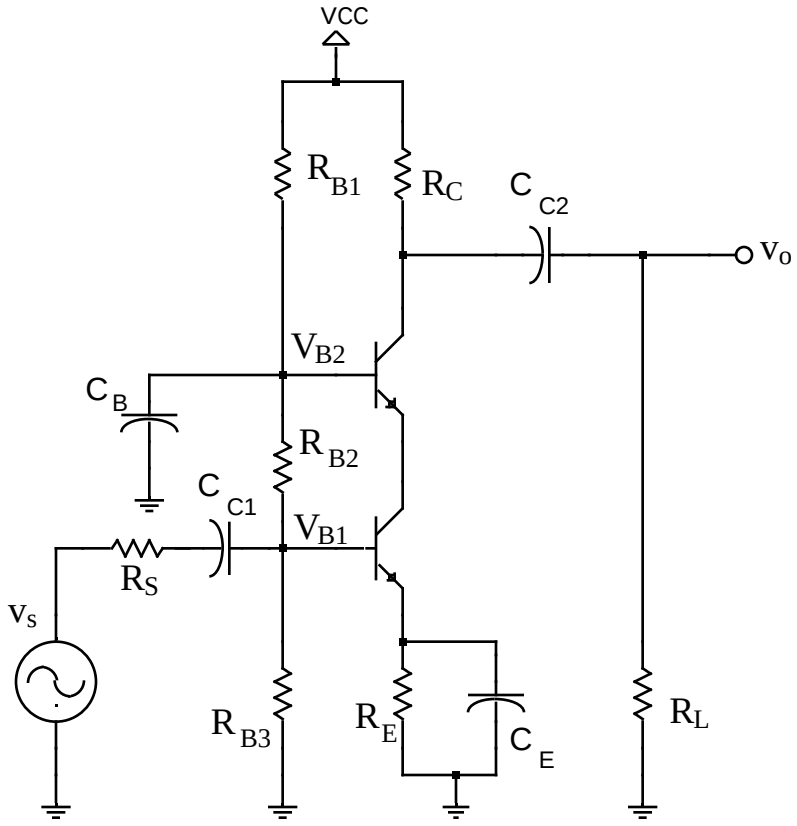
• Two comments from this:

1) The CB amplifier, despite its very low input impedance (≈ r_e), has very good high-frequency response.

2) The second-order transistor model effects (such as r_x) may become significant at high frequencies for the CB configuration.

6: CASCODE AMPLIFIERS = CE + CB

• This is a handy type of amplifier that is a **CE stage driving a CB stage**...



• The biasing for both stages is set up using R_{B1}, R_{B2}, and R_{B3} as a voltage divider, and R_E sets the total quiescent current in the output stage.

• In a nutshell, the CE stage's "R_C" is the input of the CB stage ($\approx r_e$) so the CE stage has a gain of about one and **no real Miller multiplication of C_μ**... the **gain comes from the CB stage.**

• It is a fast amplifier.

• The details are presented in a separate section below.

Chapter 9: THE COMMON COLLECTOR AMPLIFIER

Although we modern persons tend to take our electric lights, radios, mixers, etc., for granted, hundreds of years ago, people did not have any of them, which is just as well because there was no place to plug them in.

Dave Barry

1: OBJECTIVES

• To learn about:

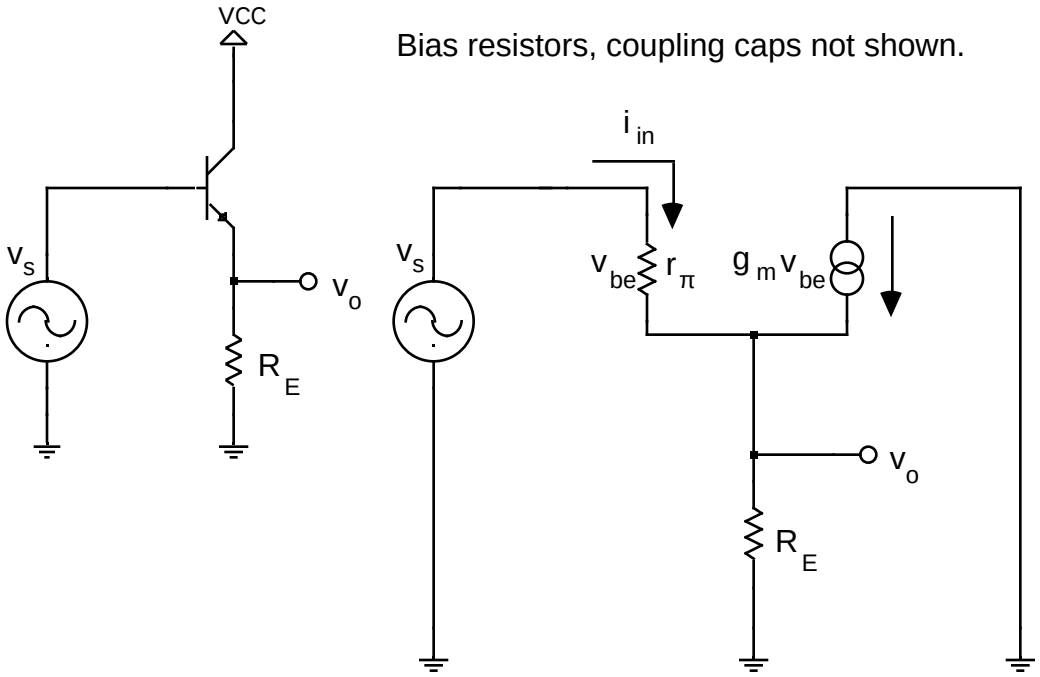
• The common collector or emitter follower BJT amplifier configuration (the last one with only one BJT in it!) in terms of “what is it good for...”

• The basic properties of the CC amplifier.

• The frequency response of the CC amplifier

READ S&S Pages 259 - 265 and S & S Section 7.8

2: COMMON COLLECTOR CIRCUIT



• We know that,

$$v_s = i_{in} r_\pi + (i_{in} + g_m v_{be}) R_E = i_{in} r_\pi + (i_{in} + g_m r_\pi i_{in}) R_E = i_{in} r_\pi + (i_{in} + \beta i_{in}) R_E$$

$$v_s = i_{in} \left[r_\pi + (\beta + 1) R_E \right]$$

• The input current is thus,

$$i_{in} = \frac{v_s}{r_\pi + (\beta + 1) R_E}$$

• Note that the extra current supplied by the g_m generator in addition to i_{in} makes R_E look like a much larger resistor in series with r_π.

• The current flowing in the collector circuit is

$$g_m v_{be} = \beta_F i_b$$

• Therefore, the output voltage is given by,

$$v_o = (\beta + 1) i_{in} R_E = \frac{(\beta + 1) R_E}{r_\pi + (\beta + 1) R_E} v_s$$

which gives a voltage gain of,

$$A_V = \frac{v_o}{v_s} = \frac{(\beta+1)R_E}{r_\pi + (\beta+1)R_E}$$ (in a voltage divider form)

• BUT since $(\beta_F + 1)R_E >> r_\pi$ -> $\boxed{A_V \approx 1}$

• You can also rearrange the gain equation into,

$$A_V = \frac{R_E}{\frac{r_\pi}{(\beta+1)} + R_E} = \frac{R_E}{r_e + R_E}$$

which may be a more intuitive way of looking at the "voltage divider."

• The circuit is a **"voltage follower"** or **"emitter follower"** (i.e. the emitter follows the base voltage) and is similar to the unity-gain op-amp circuit...

• **Note that the output voltage "follows" the input voltage but is always one v_{be} drop lower!!! This only matters in DC-coupled applications, that are generally not of importance here....**

• It is can be seen from

$$i_{in} = \frac{v_s}{r_\pi + (\beta+1)R_E}$$

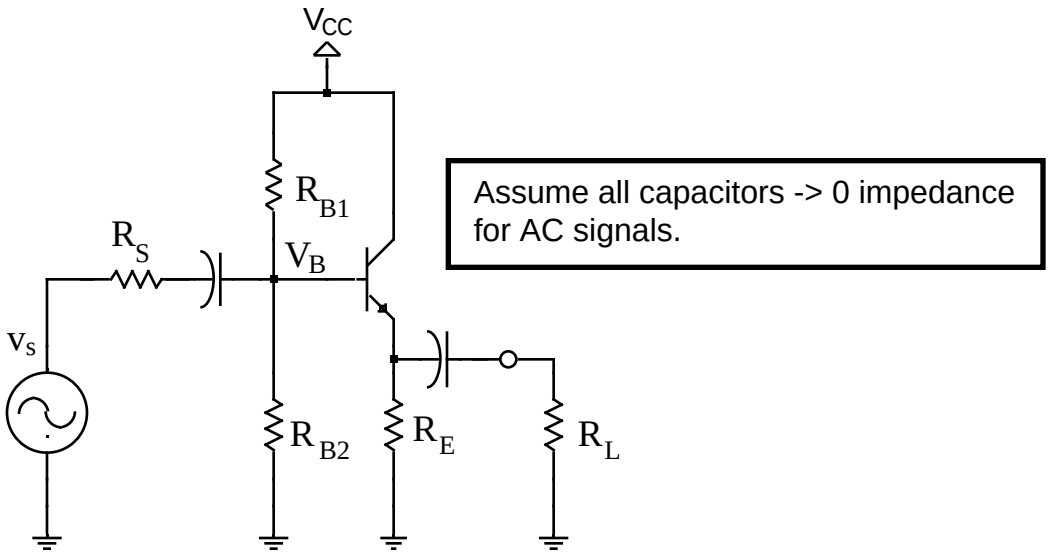
that

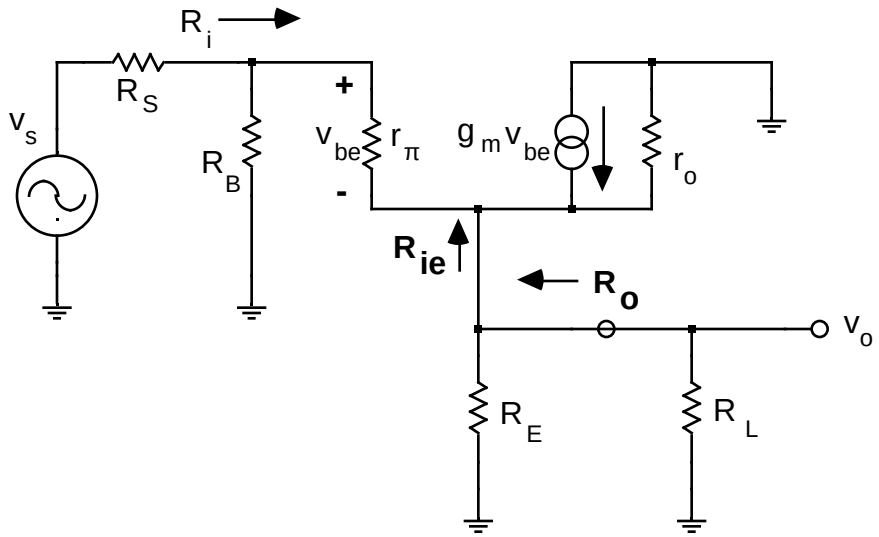
$$\boxed{R_{in} = r_\pi + (\beta+1)R_E}$$

• This is typically in the > 100 KΩ range, which is a reasonably **high input impedance.**

• Note that in Sedra and Smith (pages 259 - 265), the series resistance of the signal source, R_S, a parallel input resistance from base to ground, R_B, a load resistance R_L, and the output resistance of the transistor, r_o, are also taken into account in the derivations as shown in Fig. 4.46.

3: PRACTICAL CC CIRCUIT





• For the "full" circuit, where $R_B = R_{B1} \,||\, R_{B2}$, one obtains an input impedance of,

$$R_i = R_B \,||\, (\beta+1)\left[r_e + \left(R_E \,||\, r_o \,||\, R_L\right)\right] = R_B \,||\, \left[r_\pi + (\beta+1)\left(R_E \,||\, r_o \,||\, R_L\right)\right]$$

• The latter form can be found by inspection...

• The output resistance can be determined by replacing R_L with a test voltage source v_x and using,

$$R_O \equiv \frac{v_x}{i_x}$$

• The resistance looking into the emitter, R_{ie}, can be computed using,

$$R_{ie} \equiv \frac{v_x}{i_e}$$

$$i_e = - i_b - \beta i_b = - (1 + \beta) i_b$$

$$i_b = - \frac{v_x}{r_\pi + (R_S \,||\, R_B)}$$

• So R_{ie} is,

$$R_{ie} \equiv \frac{v_x}{i_e} = \frac{r_\pi + (R_S \,||\, R_B)}{(\beta + 1)}$$

which gives R_o (by placing R_{ie} in parallel with R_E and r_o),

$$\boxed{R_o \equiv \frac{v_x}{i_x} = R_E \,||\, r_o \,||\, \frac{r_\pi + (R_S \,||\, R_B)}{(\beta + 1)}}$$

• The voltage gain for the “full” circuit can be shown to be,

$$\boxed{A_V \equiv \frac{v_o}{v_s} = \left(\frac{R_i}{R_i + R_S}\right)\left(\frac{R_E \,||\, r_o \,||\, R_L}{r_e + [R_E \,||\, r_o \,||\, R_L]}\right) = \left(\frac{R_i}{R_i + R_S}\right)\left(\frac{[\beta + 1][R_E \,||\, r_o \,||\, R_L]}{r_\pi + [\beta + 1][R_E \,||\, r_o \,||\, R_L]}\right)}$$

• This includes a first term which takes into account the voltage division at the input and a second term where we have modified the original gain equation to take into account the fact that r_o and R_L are in parallel with R_E in the small-signal equivalent circuit.

• Again, if R_S is small, $A_V \approx 1$.... (typically what we want when we use a CC stage)

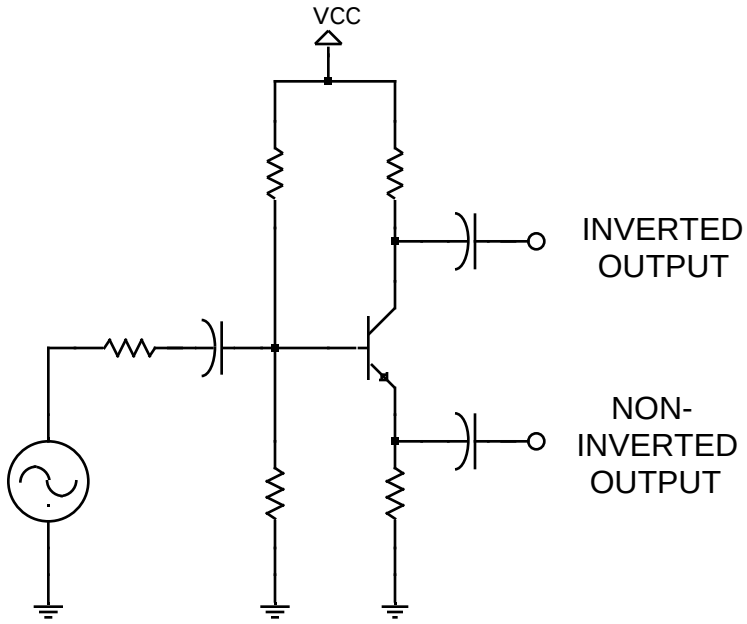
• The **current gain** is quite high, and for $R_L << (R_E \parallel r_o)$ (i.e. R_L is like a short circuit), the current gain is approximately,

$$A_i \equiv \frac{i_o}{i_i} = \frac{\frac{v_o}{R_L}}{\frac{v_s}{(R_S + R_i)}} \approx \frac{R_i}{R_L} \approx \frac{r_\pi + (\beta+1)R_L}{R_L} \approx (\beta+1)$$

• Note that the r_π/R_L term may be significant if it is large relative to (ß+1), but this is generally not the case.

• Thus, the CC amplifier can be used as a **current booster** or **voltage follower**.

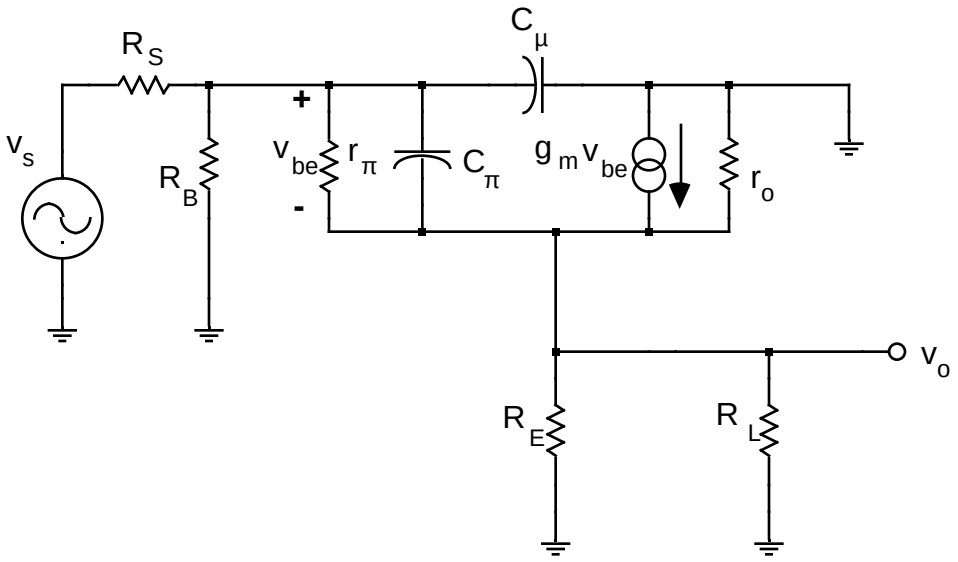
4: THE PHASE SPLITTER CIRCUIT



• This circuit gives inverted and non-inverted outputs from the same input signal... It's not really CE or CC.... Think about its operation...

5: QUICK LOOK AT CC FREQUENCY RESPONSE

• The details of the derivation are presented in S & S Section 7.8, but an overview is useful here....



• Based on a “full” analysis (See S & S), the dominant pole frequency is given by,

$$\omega_p = \frac{1}{\left[\left(R_S + r_x\right) \| \left(1 + g_m\left[R_E \| R_L\right]\right) r_\pi\right]\left(C_\mu + \frac{C_\pi}{1 + g_m\left[R_E \| R_L\right]}\right)}$$

(NOTE THAT r_x is not shown in the above AC equivalent circuit and, in fact, can typically be neglected since it is usually on the order of 10Ω... also note that R_B is considered to be very large here...)

• Practically speaking, the input pole can usually be approximated by,

$$\omega_p \approx \frac{1}{\left(R_S + r_x\right) C_\mu}$$

• An alternative is to approximate the high frequency response using the method of open-circuit time constants....

6: DESIGN OF CC STAGES

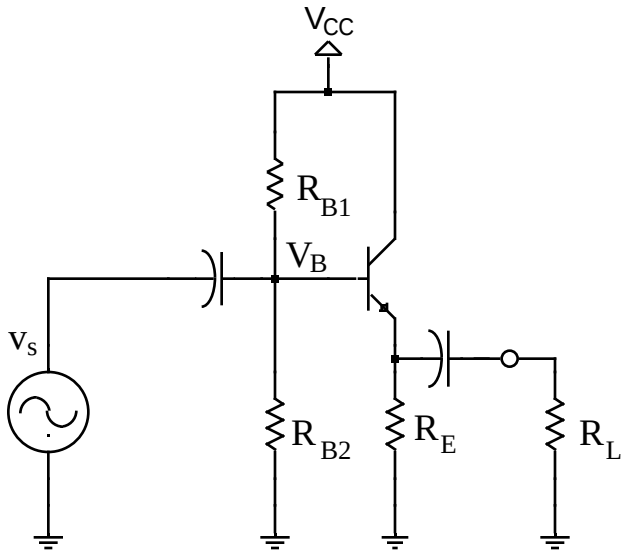
• The design process is similar to that for the other single-BJT amplifiers!

1) Assuming you need a basic follower, you don't worry about gain (unless you need a particular current gain, and then you choose a transistor with the right β).

2) You choose an I_C value that you want to operate at and calculate g_m, etc.

3) Bias stages are done the same way as before.

TYPICAL CC CIRCUIT:



Chapter 10: CASCADED AND CASCODE AMPLIFIERS

Gee Toto, I guess we're not in Terman anymore!
Stanford EE at first job interview in Silicon Valley...

1: OBJECTIVES

• To learn about:

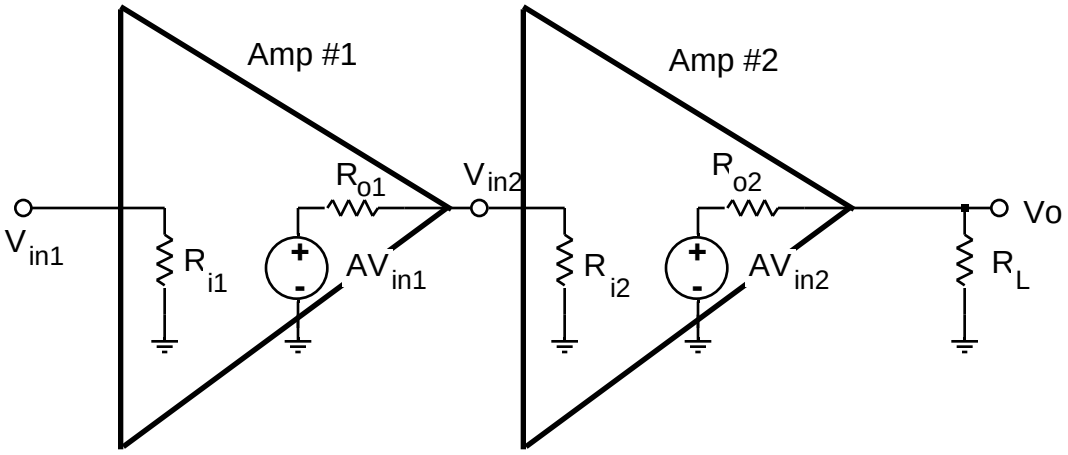
What happens when you put a bunch of amplifiers in series.... in other words, look at inter-stage loading effects (affecting gain and frequency response).

To study a very useful multi-transistor amplifier: the cascode configuration. This will combine what we know about common emitter and common base amplifiers.

READ S&S Sections 7.7, 7.8 and 6.1 - 6.3

NOTE: we will use S & S notation for $C_{BC} = C_{\mu}$ here.

2: AMPLIFIERS IN SERIES (CASCADED)



• Now it is necessary to consider what happens when amplifiers are put in series. Looking at the above example, it is clear that the input and output resistances (or impedances!) come into play by **reducing the overall gain**.

• **If the amplifiers were ideal** (R_{out} = 0 and R_{in} = ∞), and each had a gain of A, the overall gain would simply be A^2!

• In the above example, let's work out the gain assuming nothing about the R_{in} and R_{out} of each stage, looking at them as **voltage dividers** between each stage and between the last stage and the load.

• Note that in practice, impedances, Zi, would normally be used, not resistances, but they serve to illustrate the point here.

$$v_{in2} = Av_{in1}\left(\frac{R_{i2}}{R_{i2}+R_{o1}}\right)$$ <- Losses between stages and first amplification

$$v_o = Av_{in2}\left(\frac{R_L}{R_L+R_{o2}}\right)$$ <- Losses Due To R_{o2} and second amplification

$$\frac{v_o}{v_{in}} = A^2\left(\frac{R_{i2}}{R_{i2}+R_{o1}}\right)\left(\frac{R_L}{R_L+R_{o2}}\right)$$ <- Overall eqn. assuming <u>equal</u> gains (A)!

• As expected, the equation reduces to the ideal case of $A_V = A^2$ for two identical stages if we let the R_o's go to 0 and the R_i's go to infinity.

• The above equations assume that the individual amplifier gains ("A") do not change with output loading.

• For most op-amps since R_{in} = MΩ to GΩ range, and R_o ≈ 50 - 100 Ω, the gains are pretty close to being A^N (where N = number of equal-gain stages).

• Just to check that, assume a "not-so-hot" op-amp with R_o = 100Ω and R_{in} = 1MΩ, what is the gain with two stages of gain A in series? (assume R_L = 1 MΩ too)

$$\frac{v_o}{v_{in}} = A^2 \left(\frac{1M\Omega}{1M\Omega+100\Omega}\right)\left(\frac{1M\Omega}{1M\Omega+100\Omega}\right) = A^2\,(0.9999)\,(0.9999) = 0.9998\,A^2$$

• That is pretty close to A^2!

• In fact, you would have to go to a **ONE HUNDRED** stages with these specifications before you even lost 1% of the expected "ideal" gain (i.e. to get 0.99 A^{100})...

• By the time you reached that point, other effects would have caused much more trouble (for example, the fact that noise from each successive stage is added to the noise coming into that stage and amplified... on down the line!).

• There are practical reasons why you just can't continue cascading stages "forever..."

If DC-coupled, real-world offsets can be impossible to trim out!

Even if AC-coupled, noise from preceding stages gets amplified by each downstream amplifier stage, making for nothing but a noise source after a while!

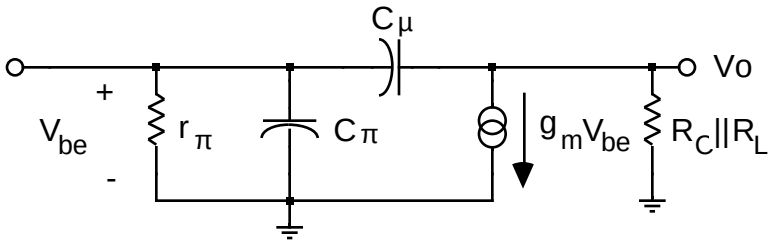
• We normally refer all noise to the **input** of an amplifier, taking out the effects of the gain stages.

3: THE CASCODE AMPLIFIER

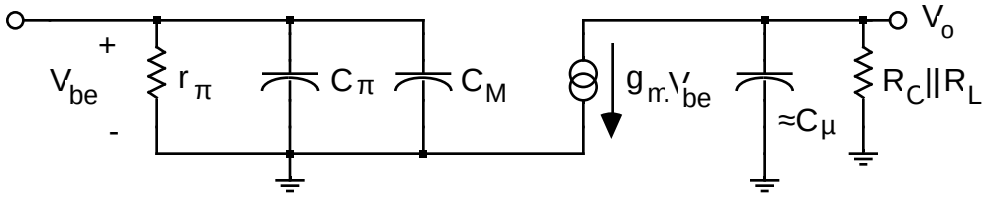
• Now... how do we make a fast amplifier (i.e. for oscilloscopes, etc.)?

• **The idea:** Combine the advantages of common emitter (high R_{in}) with common base (no Miller effect) to get greatly improved performance.

• Remember that the CE amplifier suffers the most from the roll-off caused by the input pole.



BECOMES ...



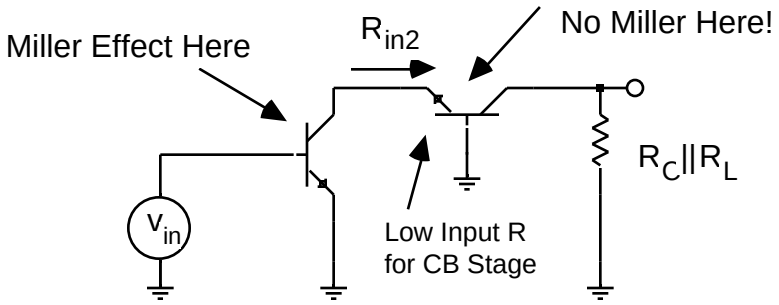
where the Miller Capacitance is $C_M = C_\mu \left(1+g_m R_C||R_L\right)$

(Note that C_μ is just another notation for C_{BC}.)

• The cascode amplifier is a CE amplifier driving a CB stage.

• The CE stage, where the Miller Effect could be a problem, is **deliberately set up for a low gain** to minimize it!

• The gain is obtained from the CB output stage, not the CE stage.



• Let's look at the Miller capacitance at the CE stage... First figure out what the "R_C" of the CE stage is (the input of the CB stage!).

• Remember the input resistance of a common-base amplifier is,

$$R_{in2} \approx r_e \approx \frac{1}{g_{m2}}$$

• Now we can calculate the CE gain and substitute into the Miller equation (remember that we multiply the capacitance by [1 - A_V], where A_V is the voltage gain),

$$C_M = C_\mu\left(1 + g_m R_C \parallel R_L\right) \approx C_{\mu 1}\left(1 + g_{m1}\frac{1}{g_{m2}}\right)$$

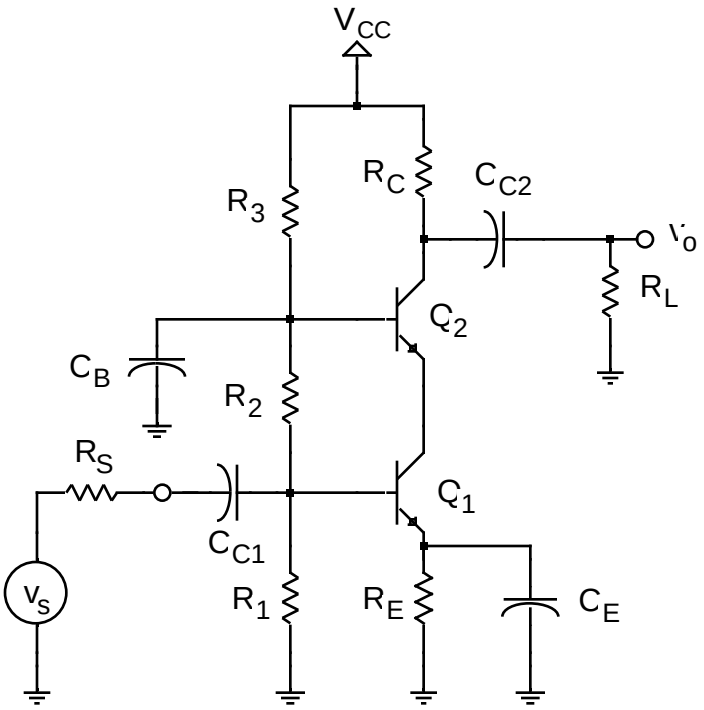
(Note that r_o of the transistors is neglected here, and would appear in parallel with R_C and R_L if considered.)

• If $g_{m1} = g_{m2}$, then,

$$C_M \approx C_{\mu 1}(1+1) = 2C_{\mu 1}$$

• Thus the Miller Effect is minimized in this configuration and the CE gain is ≈ -1.

4: PRACTICAL CASCODE AMPLIFIER CIRCUIT



• One can use a "1/4, 1/4, 1/4, 1/4" biasing scheme here, where V_{B1} is 1/4 V_{cc}, V_{B2} is 1/2 V_{cc} and so on.

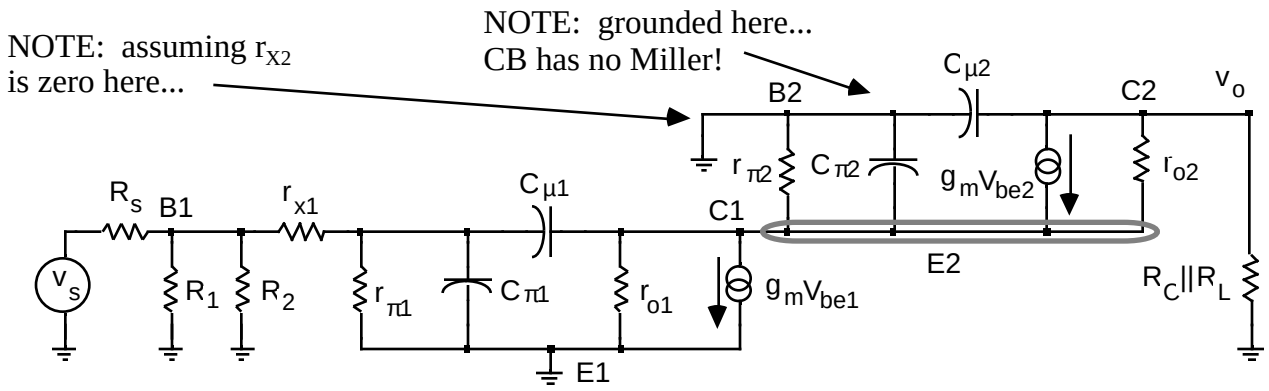
• R_E sets the current through **BOTH** Q_1 and Q_2. **In fact, if the ß values are relatively large, you can assume that the collector currents are equal...**

$$I_{E1} = \frac{\beta + 1}{\beta} I_{C1} \approx I_{C1}$$

$$I_{E1} \approx I_{C1} = I_{E2} \approx I_{C2}$$

• R_1, R_2, and R_3 set the bias points, and R_E can be used to adjust the current through both transistors.

The AC Equivalent Circuit (High Frequency)

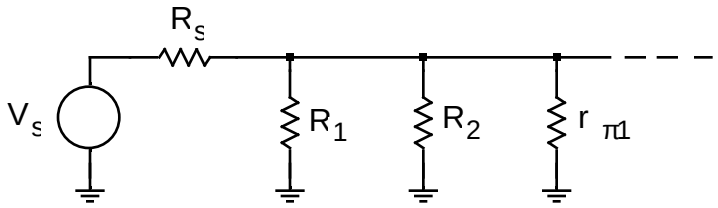


4.1 THE INPUT SECTION

• Assuming $r_{x1} = 0$ (See S&S p. 534)...

• As is usually the case, the input resistances just act as a voltage divider...

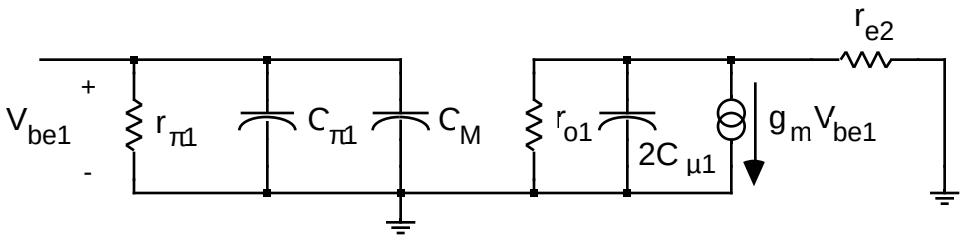
$$v_{be1} = v_s \left(\frac{r_{\pi 1} \,||R_1||\, R_2}{R_S + r_{\pi 1} \,||R_1||\, R_2} \right)$$



4.2 THE COMMON EMITTER STAGE

• The CE amplifier output is looking at r_{e2}.

$$C_M = C_{\mu 1}\left(1+g_{m1}r_{e2}\right) = 2\, C_{\mu 1} \quad \text{if} \quad r_{e2} \approx \frac{1}{g_{m2}} = \frac{1}{g_{m1}} \quad \text{and} \quad r_{o1}=\infty$$

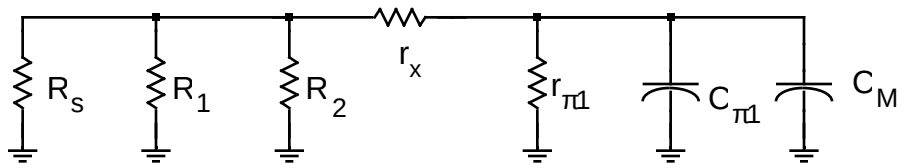


• We know that the gain for a non-emitter-degenerated CE stage (note that R_E is bypassed by C_E!) is,

$$A_V = - g_{m1} \left(R_C \parallel R_L \right)$$

and that here, $R_C \parallel R_L$ is simply r_{e2}... the CE GAIN ≈ -1 in this case.

INPUT TIME CONSTANT FOR THE CE STAGE



$$C_M = 2C_{\mu 1}$$

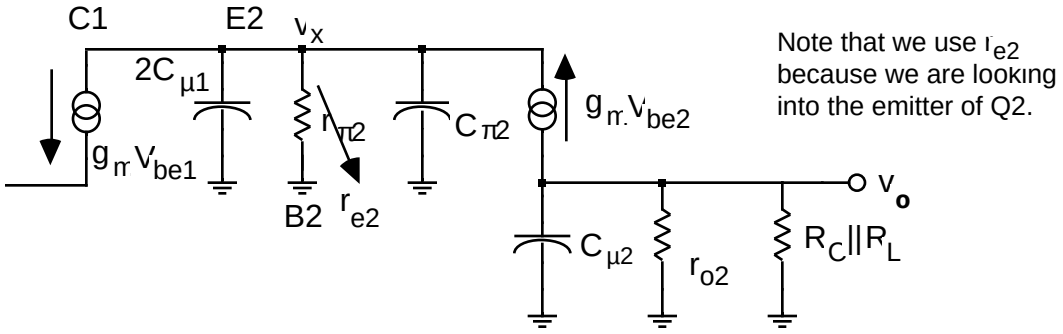
$$\omega_1 = \frac{1}{\left[\left(R_S \parallel R_1 \parallel R_2 + r_{x1} \right) \parallel r_{\pi 1} \right] \left(C_{\pi 1} + 2C_{\mu 1} \right)} \approx \frac{1}{\left(R_S \parallel R_1 \parallel R_2 \parallel r_{\pi 1} \right) \left(C_{\pi 1} + 2C_{\mu 1} \right)}$$

• Note that the latter approximation assumes $r_x \approx 0$, but if R_s is very small, r_x may be significant (otherwise, the input pole theoretically goes to infinite frequency).

4.3 THE COMMON BASE STAGE

• Now look at the CB Stage to get the overall gain...

• Since the base is grounded, the non-grounded half of $C_{\pi 2}$ must look at $r_{\pi 2}$ "through the emitter."



• It is known that since the gain of the CE stage is ≈ -1, $V_x \approx -V_s$.

• We know that the gain of CB amplifier is,

$$A_{VCB} = \frac{v_o}{v_x} = +g_{m2}\left(r_{o2} \,||\, R_C \,||\, R_L\right) \approx g_{m2}\left(R_C \,||\, R_L\right)$$

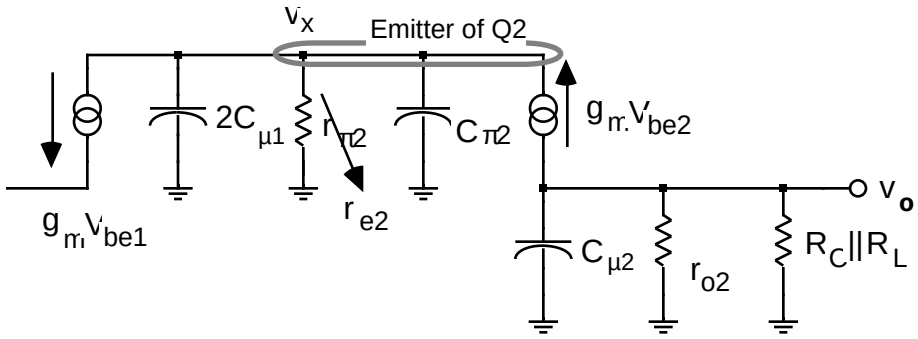
• We can thus write the complete midband gain (neglecting r_x and r_o) as:

$$A_V \equiv \frac{v_o}{v_s} = \underbrace{\left(\frac{r_{\pi 1} \,||\, R_1 \,||\, R_2}{R_S + r_{\pi 1} \,||\, R_1 \,||\, R_2}\right)}_{\text{Input Divider}} \underbrace{(-1)}_{\text{CE stage}} \underbrace{g_{m2}\left(R_C \,||\, R_L\right)}_{\text{CB stage}}$$

4.4 THE OTHER TIME CONSTANTS

• So far, we only found one time constant (the input) so, let's find the others, in **between stages** and at the **output**...

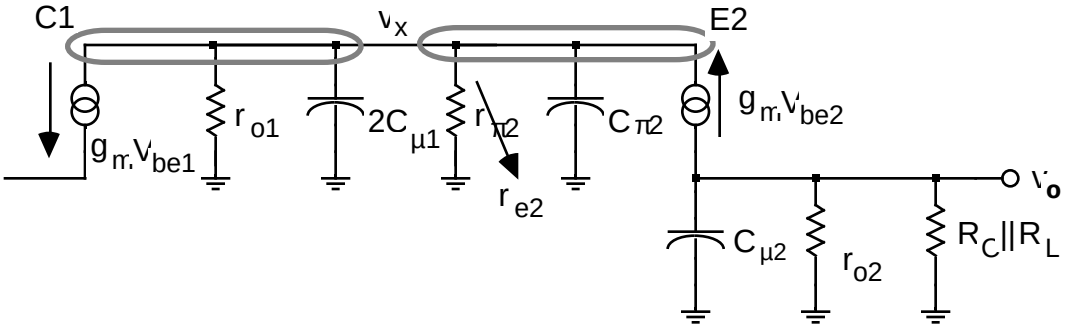
• In between the stages...



$$\omega_2 = \frac{1}{C_{\pi 2} r_{e2}}$$

• **NOTE: Use r_e not r_π because we are looking into Q_2's emitter!!!**

• Note that we could also consider two less-important components in between stages, r_{o1} and $C_{\mu 1}$ ($C_{\mu 1}$ appears at the output because of the Miller Effect)...



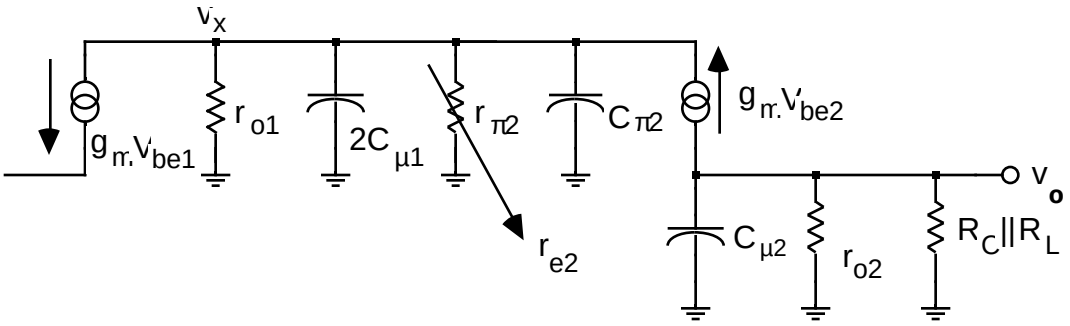
• You will note that sometimes these other two components are considered, other times they are not (particularly in the text book!). Since it is relatively easy to consider them, you can include them OR show that they don't change things much (i.e. $C_{\mu 1} << C_{\pi 2}$ and $r_{e2} << r_{o1}$). The "complete" equation would be,

$$\omega_2 = \frac{1}{\left(C_{\pi 2} + 2C_{\mu 1}\right)\left(r_{e2} \parallel r_{o1}\right)}$$

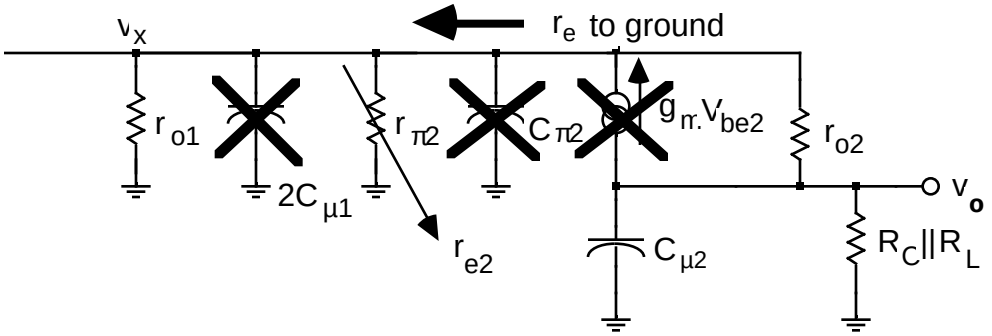
• r_{o1} is typically ≈ 100 KΩ and r_{e2} is typically a few Ohms, so r_{e2} typically determines the net resistance. You may have to look at $C_{\pi 2}$ and $C_{\mu 1}$ to decide...

• This inter-stage time constant typically corresponds to a very high frequency. Its value doesn't depend on R_s or the Load (R_L).

• The **output stage** time constant...



• Note that r_{o2} is shown with one end grounded to simplify the analysis, but the circuit actually would be something like ($C_{\mu 1}$ and $C_{\pi 2}$ are shown as open-circuits as well as the current source),



• Effectively, you have r_{o2} connected to a very small resistance (r_e) to ground, so we can just look at it as having one end grounded as shown above (i.e. $r_{o2} + r_e \approx r_{o2}$).

$$\omega_3 = \frac{1}{C_{\mu 2}\left(r_{o2}||R_C||R_L\right)} \approx \frac{1}{C_{\mu 2}\left(R_C||R_L\right)}$$

• Now recall the input pole...

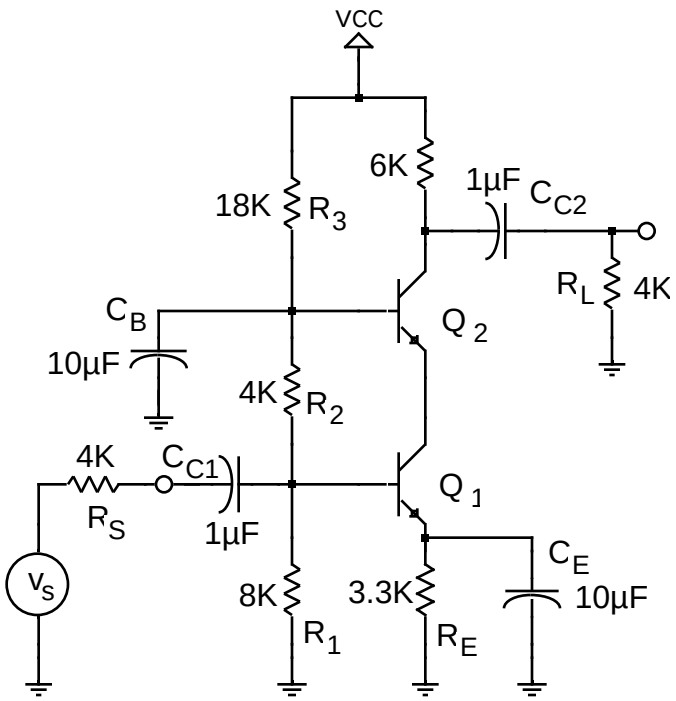
$$\omega_1 = \frac{1}{\left(R_S||R_1||R_2||r_{\pi 2}\right)\left(C_{\pi 1}+2C_{\mu 1}\right)}$$

• If R_s is large, this frequency is lower than ω_2 and ω_3 ...

• So, like the CE stages alone, the **input** pole **typically *(but not always!)*** determines f_H, but here there is only a 2X Miller multiplication!

5: QUICK CASCODE EXAMPLE

(S&S EX 7.20, p. 536)



• Given : V_{cc} = +15 V, $I_E \approx$ 1mA, $Q_1 = Q_2$ (identical devices), ß = 100

• Doing the analysis is not a big problem ...

$$r_\pi = \frac{ß}{g_m} = 2.56\ K\Omega$$

$$g_m \approx \frac{I_C}{V_T} = \frac{1mA}{25.9} = 0.039\ \Omega^{-1}$$

$$A_M = -\left(\frac{R_\pi||R_1||R_2}{R_S + R_\pi||R_1||R_2}\right) g_m \left(R_C||R_L\right) = -23.1$$

$$f_1 = \frac{\omega_1}{2\pi} = \frac{1}{2\pi} \frac{1}{\left(R_S||R_1||R_2||r_{\pi 2}\right)\left(C_{\pi 1}+2C_{\mu 1}\right)} = 8.75\ MHz$$

$$f_2 = \frac{\omega_2}{2\pi} = \frac{1}{2\pi} \frac{1}{C_{\pi 2} r_{e2}} = \frac{1}{2\pi} \frac{1}{\left(13.9\ pF\right)\left(25.6\Omega\right)} = 447\ MHz$$

$$f_3 = \frac{\omega_3}{2\pi} = \frac{1}{2\pi C_{\mu 2}\left(R_C \| R_L\right)} = \frac{1}{2\pi\left(2\ \text{pF}\right)\left(4\text{K} \parallel 6\text{K}\right)} = 33.2\ \text{MHz}$$ <- neglect r_o

• Clearly, f_1 is the lowest!

• Now, what if we let R_s go to 50Ω (typical for signal generators)...

f_1 goes way up (around 700 MHz) and the output pole (f_3) dominates in this case!

• The message here is ***DON'T ASSUME*** you know which pole is dominant !!!!

$$f_H = \frac{1}{\sqrt{\frac{1}{f_1^2} + \frac{1}{f_2^2} + \frac{1}{f_3^2}}} = 8.46\ \text{MHz}$$

• Compare this to the previous CE example!

A_V = -23.1

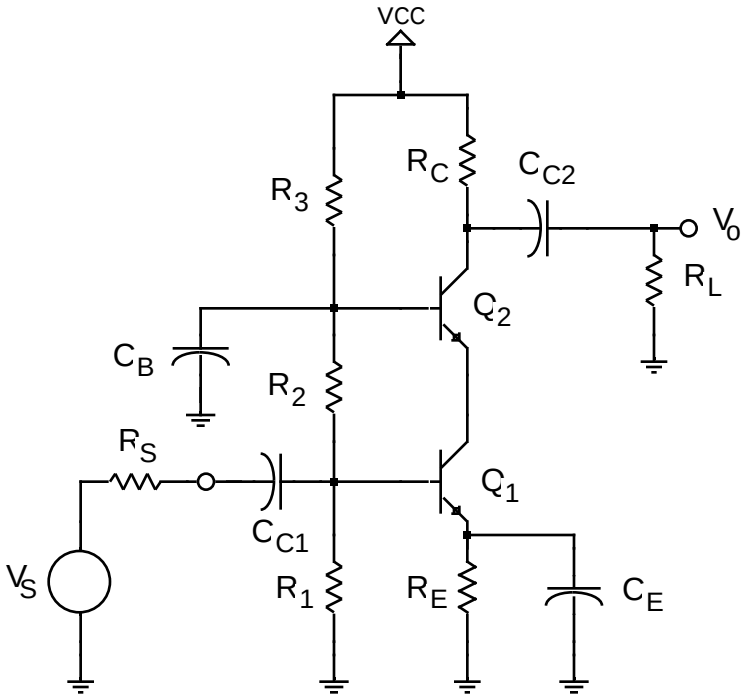
f_H = 800 KHz

6: CASCODE AMPLIFIER DESIGN EXAMPLE

• This example is analogous to the Common-Emitter design done previously in the notes. The purpose is for you to compare the two designs for differences in characteristics.

Specifications:

DC power dissipation: P_D < 25 mW
Power Supply: 12 VDC
Voltage Gain: -50X
Load: Resistive, 50 KΩ
Assume R_s = 0 Ω
Must use 2N2222A Transistors (NPN, ß = 150 measured)



All capacitors are large (100 µF) so they are essentially short-circuits for AC

Key point: The collector-emitter current running through Q_2 is assumed to be equal to that through Q_1. Further, the total power dissipation (DC, or quiescent) and the voltage gain are both determined by the choice of this current.

DESIGN PROCESS:

1) Pick V_{cc} unless specified.

V_{cc}= 12 VDC

2) Calculate I_{max}.

$$I_{MAX} = \frac{\text{Max DC Power}}{Vcc} = \frac{25\text{ mW}}{12\text{ V}} = 2.083\text{ mA}$$

3) Select an $I_C < I_{MAX}$ and solve for g_{m2}.

Let I_C = 1.8 mA

$$g_{m2} = \frac{1.8\text{ mA}}{0.0259\text{ V}} = 0.0695\ \Omega^{-1}$$

4) Let R_S = 0 or be too small to matter (for now) and solve for R_C:

$$A = -\,g_{m2}\left(R_C \| R_L\right)\left(\frac{r_\pi \| R_1 \| R_2}{R_S + r_\pi \| R_1 \| R_2}\right) \qquad R_C = \left(\frac{g_{m2}}{-A} - \frac{1}{R_L}\right)^{-1}$$

R_C = 730 Ω

5) Use a 1/4, 1/4, 1/4, 1/4 biasing rule to set up bias resistors. Let V_{CE} of the transistors = V_{cc}/4 = 3V and solve the following for R_E.

$$R_E = \frac{V_{B1} - V_{BE}}{I_E} = \frac{\frac{V_{CC}}{4} - 0.7}{I_C\,\frac{ß + 1}{ß}} = \frac{3 - 0.7}{0.001812} = 1.27\text{ kΩ}$$

6) The required base current is:

$$I_B = \frac{I_C}{ß} = \frac{0.0018}{150} = 0.012\text{ mA}$$

7) Solve for the biasing resistors.

$$I_{BIAS} > 0.1I_E \approx 0.1I_C$$

$$R_{BNET} = R_1 + R_2 + R_3 = \frac{V_{CC}}{0.1I_C} = \frac{12\text{ V}}{(0.1)(1.8\text{ mA})} = 66.7\text{k}\Omega$$

$$V_{B1} = \frac{V_{CC}}{4} = V_{CC}\,\frac{R_1}{R_1 + R_2 + R_3}$$

$$R_1 = \frac{R_{BNET}}{4} = 16.7\text{ k}\Omega$$

$$V_{B2} = \frac{V_{CC}}{2} \qquad R_2 = R_1$$

$$R_3 = 2R_1 = 2R_2 = \frac{R_{BNET}}{2} = 33.3\ k\Omega$$

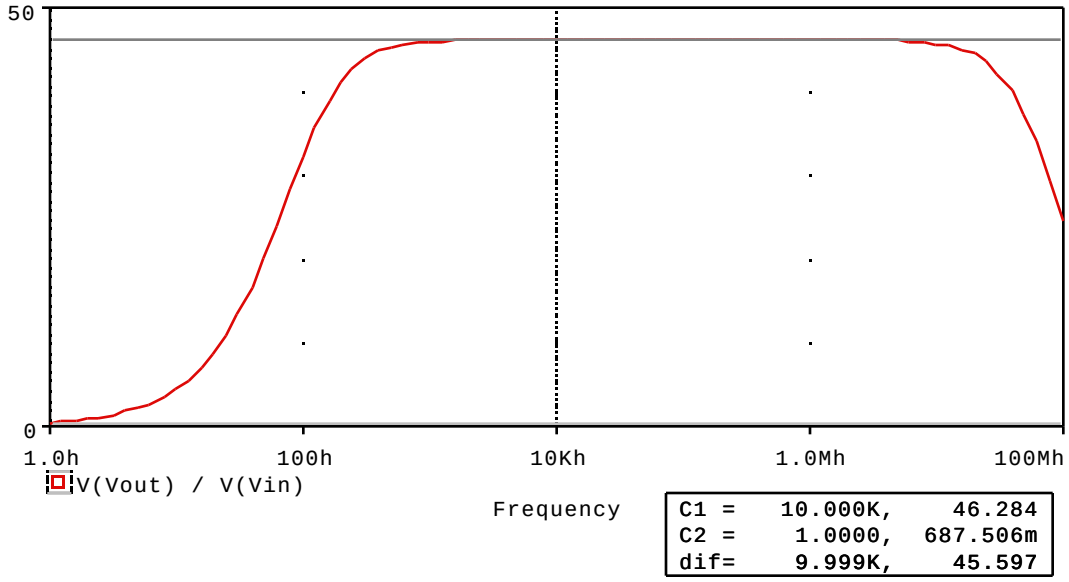
8) Now check that any R_S that may be present should not have a major impact on the gain....

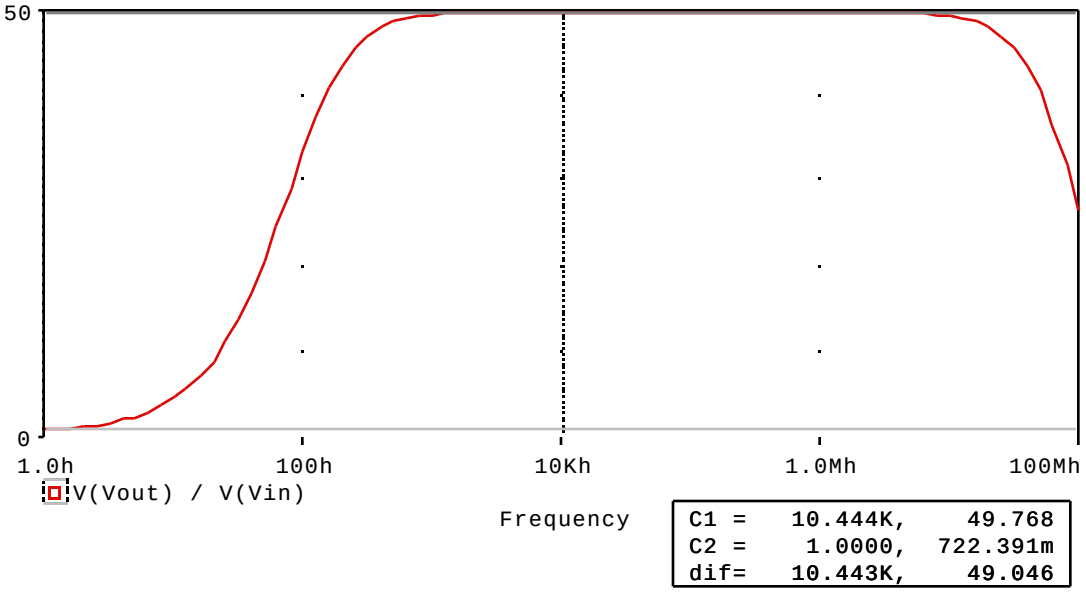
- **If little or no impact, move on.**
- **If much impact, tweak I_C and iterate if necessary.**

9) SIMULATE THE CIRCUIT ON SPICE USING THE FOLLOWING VALUES:

R_1 = 15 KΩ R_2 = 15 KΩ R_3= 30 KΩ
R_C = 750 Ω R_E = 1.3 KΩ

```
EE113 Demo - Cascode Amplifier
*Resistors
R1   VB1  0         15K
R2   VB2  VB1       15K
R3   VCC  VB2       30K
RC   VCC  VC2       750
RE   VE1  0         1.3K
RS   Vin  VX        1
RLL  Vout 0         50K
*Capacitors
C1   VX   VB1       100UF
C2   VB2  0         100UF
C5   VE1  0         100UF
C6   Vout VC2       100UF
*Sources
Vcc  VCC  0         12
Vss  0    Vin       AC 10mV
*Transistors
Q1   V01  VB1  VE1  TRANSMODEL
Q2   VC2  VB2  V01  TRANSMODEL
.MODEL  TRANSMODEL NPN (BF=150 IS=1.3E-14
+ TF=.9N CJE=6P CJC=5P)
*input frequency sweep
.AC DEC 10 1 100MEG
.PROBE
.end
```


50
0
1.0h
100h
10Kh
1.0Mh
100Mh
V(Vout) / V(Vin)
Frequency
C1 = 10.000K, 46.284
C2 = 1.0000, 687.506m
dif= 9.999K, 45.597


50
0
1.0h
100h
10Kh
1.0Mh
100Mh
V(Vout) / V(Vin)
Frequency
C1 = 10.444K, 49.768
C2 = 1.0000, 722.391m
dif= 10.443K, 49.046

Chapter 11: DIFFERENTIAL AMPLIFIERS

Ow! That's hot!
EE122 student's first encounter with a soldering iron...

1: OBJECTIVES

• To consider:

The basic idea of the differential pair.

The benefits of the differential pair (no coupling caps -> DC response, etc.).

DC operation of the differential pair.

The basic small-signal equivalent circuit for the differential pair.

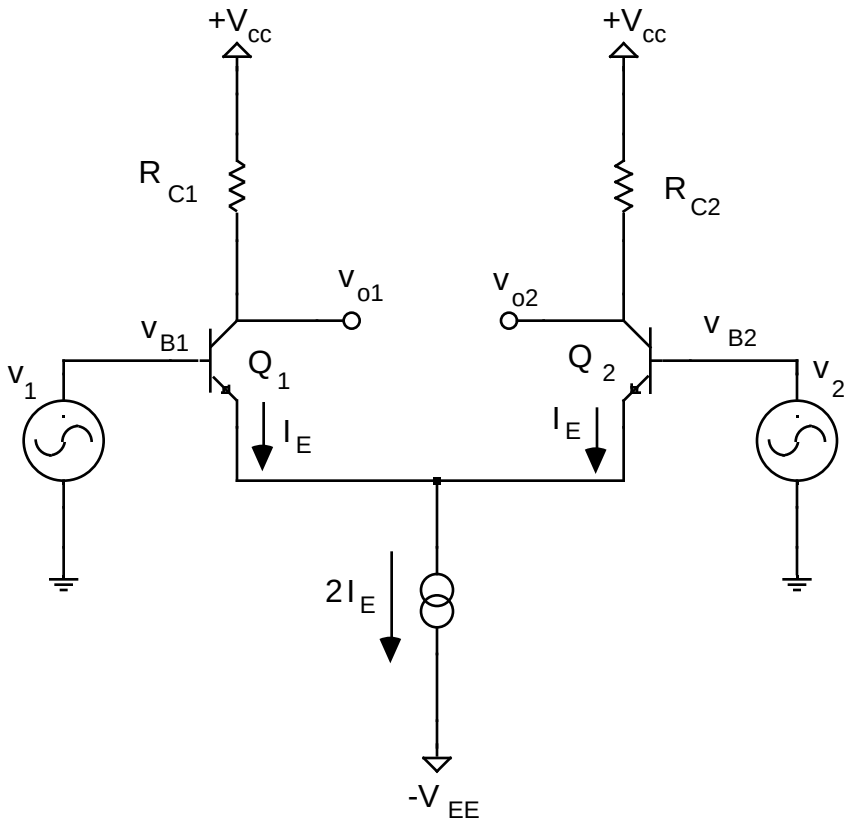
Common-mode operation of the differential pair.

The frequency response of the differential pair.

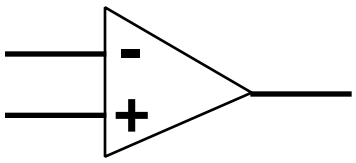
Non-ideal properties of the differential pair.

READ S&S Sections 6.1 - 6.3, 7.10 and 7.11

2: DIFFERENTIAL AMPLIFIER BASIC CONCEPTS



• The differential amplifier circuit (as shown above, it is often referred to as a differential pair) is the basis for any operational amplifier (you can find one on the input of nearly any op-amp type chip). The two transistors are ideally identical and are generally assumed to be below.



• There are two inputs, v_1 and v_2, and one can apply inputs to both (differentially) or ground one and use the amplifier in a single-ended (ground referenced) way.

• This circuit can compute the difference between two input signals.

• While the op-amp symbol ("triangle") has only one output, the differential pair shown above has two (v_{o1} and v_{o2}). One can take outputs from both (differentially) or use just one relative to ground (as you would with a typical op-amp).

• The differential pair is basically *two common emitter amplifiers* sharing a common current source that sets the *total* DC bias current through both transistors at $2I_E$. In

seeking to understand its operation, we will begin by looking at the shifting of this DC current between the two transistors when there is a large-signal imbalance between their two inputs (i.e. the difference between v_1 and v_2 is large).

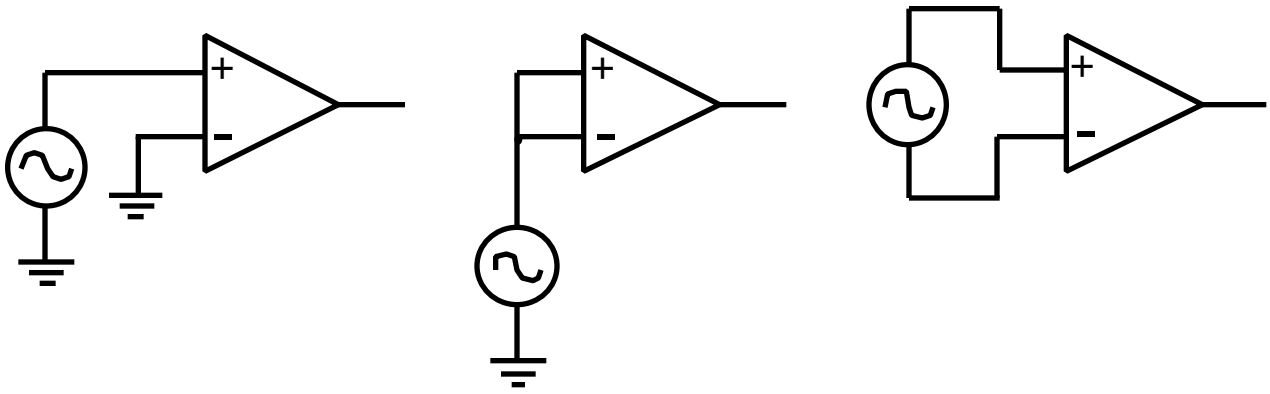
• With **NO** differential signal input (v_1 and v_2 are the same), the current flowing out the emitter of each transistor is I_E and therefore, $v_{o1} = v_{o2}$ in this situation (if $R_{C1} = R_{C2}$, which is usually the case).

• For the small-signal case, if the collector currents are the same in both transistors ($I_E \approx I_C$), their g_m's and other parameters will be equal (both transistors are as close to identical as possible).

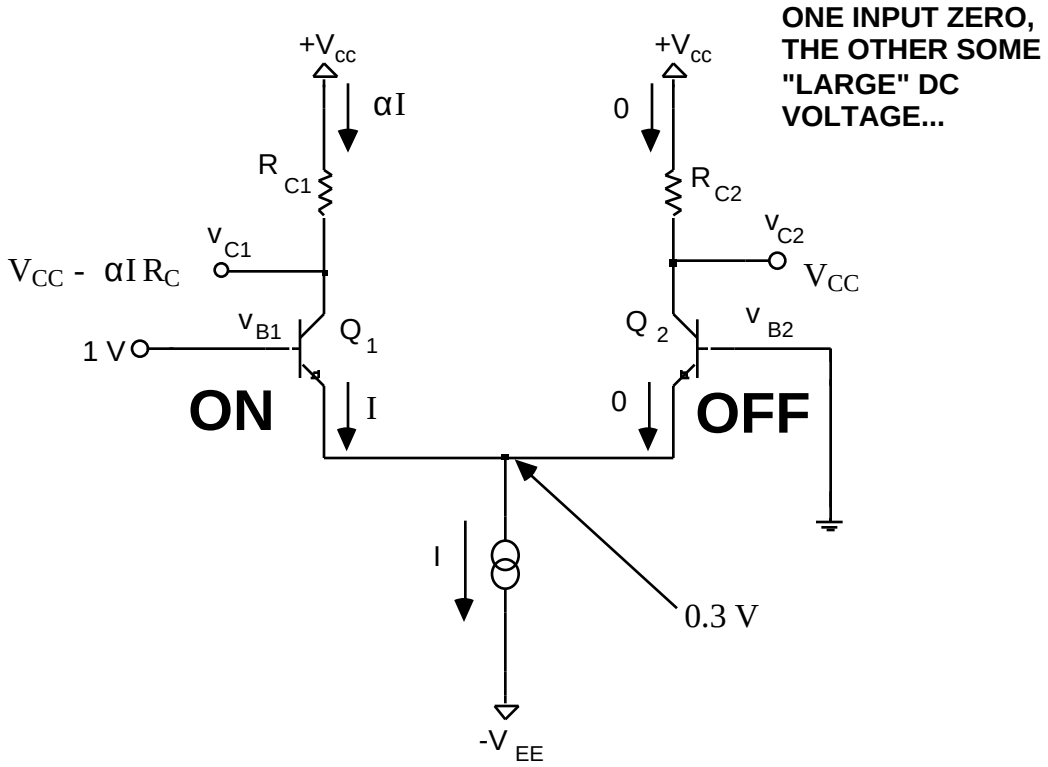
• As will be seen when the circuit is studied more closely, its symmetry is what gives rise to its "special" properties.

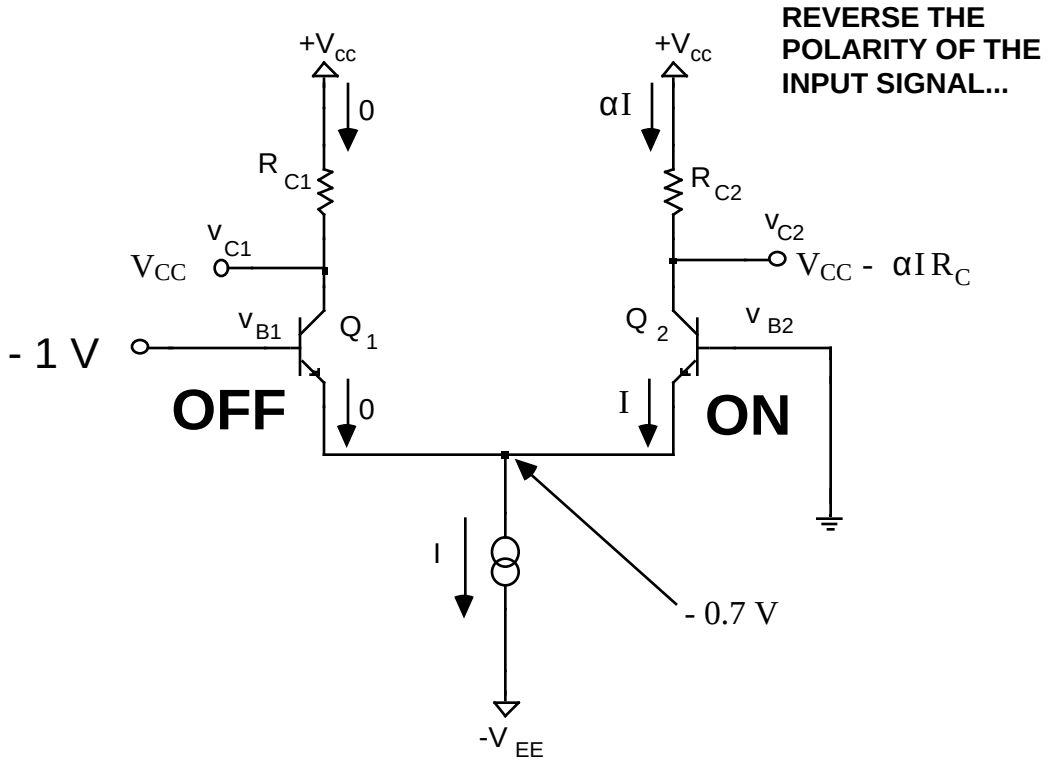
3: MODES OF OPERATION OF THE DIFFERENTIAL PAIR

Single-Ended Mode **Common Mode** **Differential Mode**



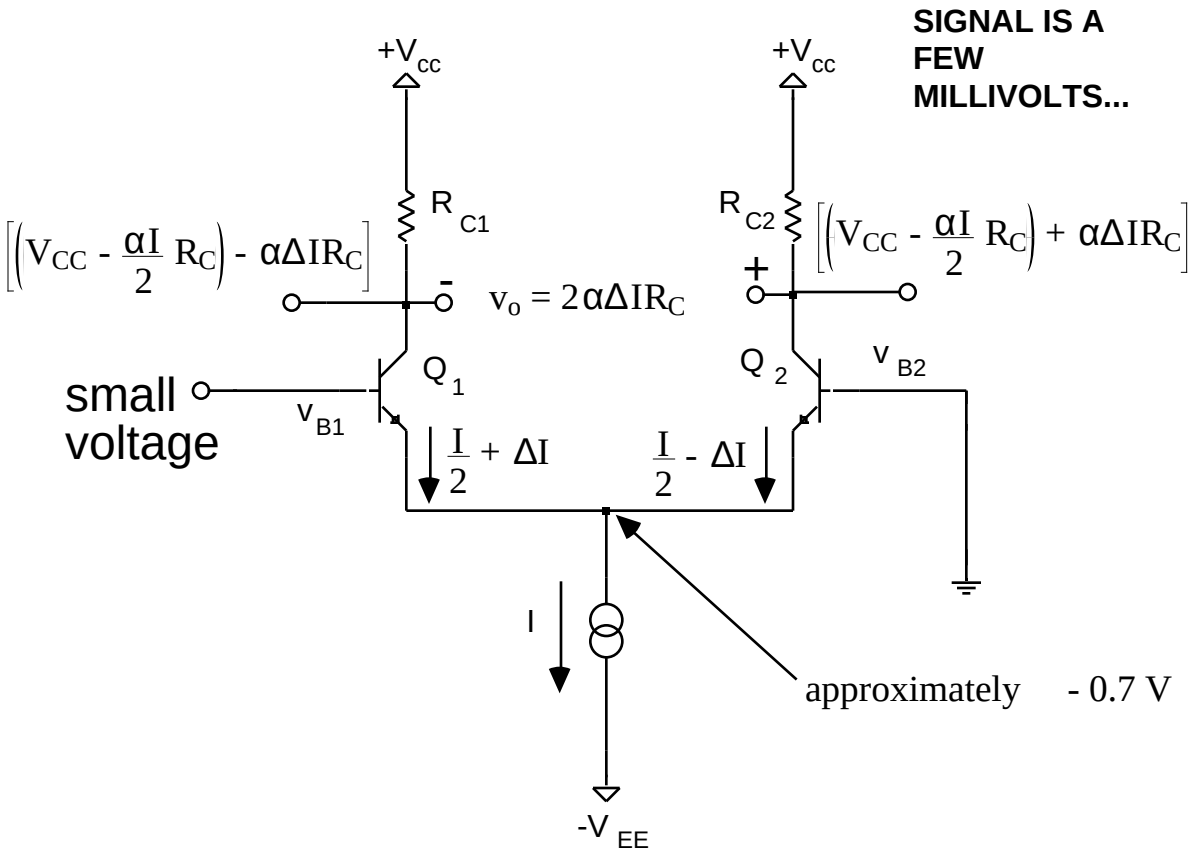
3.1 LARGE SIGNAL OPERATION





Note: single-ended operation shown.

3.2 SMALL-SIGNAL OPERATION



Note: single-ended operation shown.

• For a small input signal (this is like our previous example with one input grounded), the current distributes itself between the transistors so that one gets an incremental amount ΔI more and the other one gets ΔI less....

• **NOTE** that the differential output voltage is,

$$v_o = 2\alpha\Delta I R_C$$

• **NOTE** the polarity of v_o...

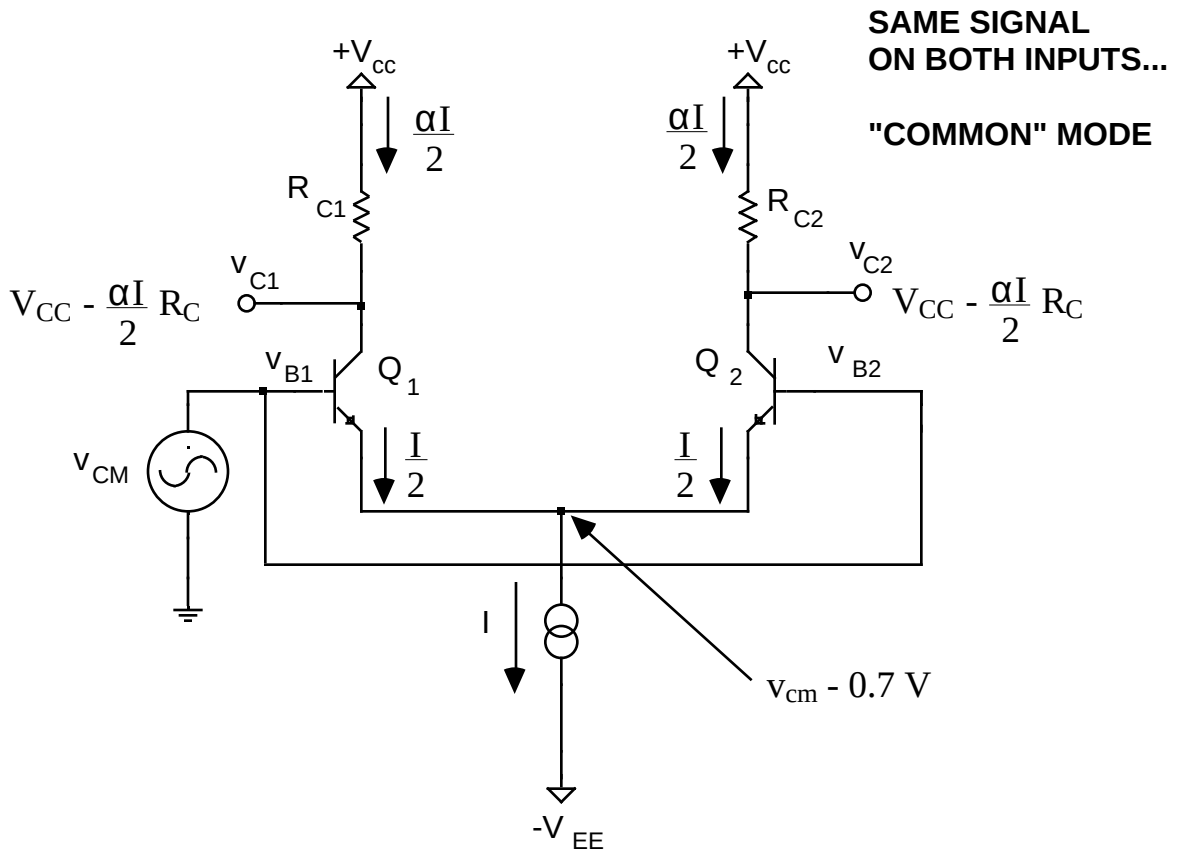
For a **POSITIVE** small input voltage, v_{C1} **DECREASES**

For a **NEGATIVE** small input voltage, v_{C1} **INCREASES**

v_{C2} does the opposite....

• **NOTE** that the current source node is at approximately -0.7V

3.3 COMMON-MODE OPERATION



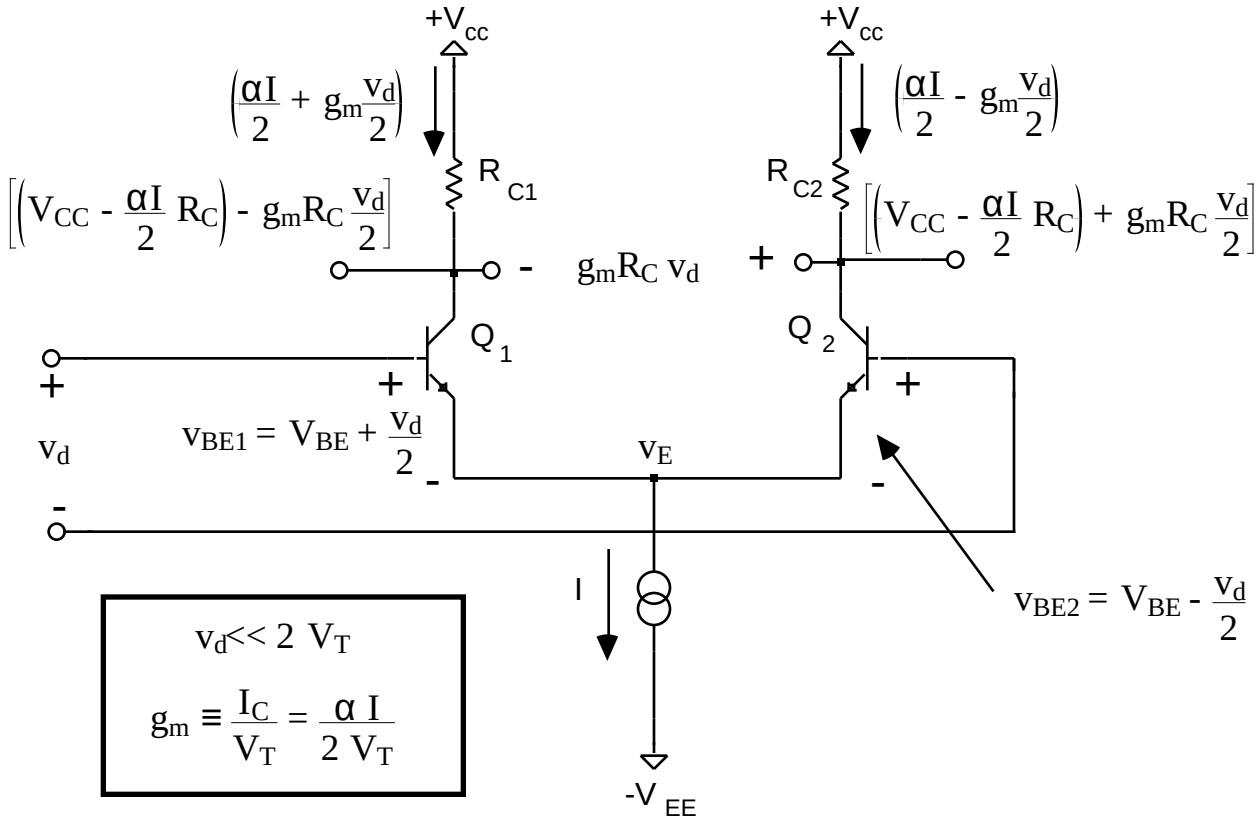
• Both inputs are driven by the *same signal* in common-mode operation.

• Since both transistors are the same (matched), the current will remain symmetrical between the two transistors and so the output voltages v_{C1} and v_{C2} will exactly track each other. Therefore **the difference between v_{c1} and v_{c2} will be ZERO.**

• This means that **common mode signals are rejected! (as long as $R_{c1} = R_{c2} = R_c$)**

• Remember from the op-amp section that common-mode rejection is supposed to be high.

4: DETAILS OF SMALL-SIGNAL OPERATION



• In this section, the goal is to look at small signal operation with differential inputs, which are seen to be split evenly between the two transitors BE junctions.

• By defining the voltage at the common emitter node as v_E and taking note of the polarities shown above, one can write expressions for the emitter currents in terms of a common voltage...

$$i_{E1} = \frac{I_S}{\alpha} e^{\frac{(v_{B1} - v_E)}{v_T}} \qquad i_{E2} = \frac{I_S}{\alpha} e^{\frac{(v_{B2} - v_E)}{v_T}}$$

• Which can be combined into,

$$\frac{i_{E1}}{i_{E2}} = e^{\frac{(v_{B1} - v_{B2})}{v_T}}$$

• Remember that $I_C = I_S e^{\frac{v_{BE}}{v_T}}$

• These equations can be rearranged into the forms,

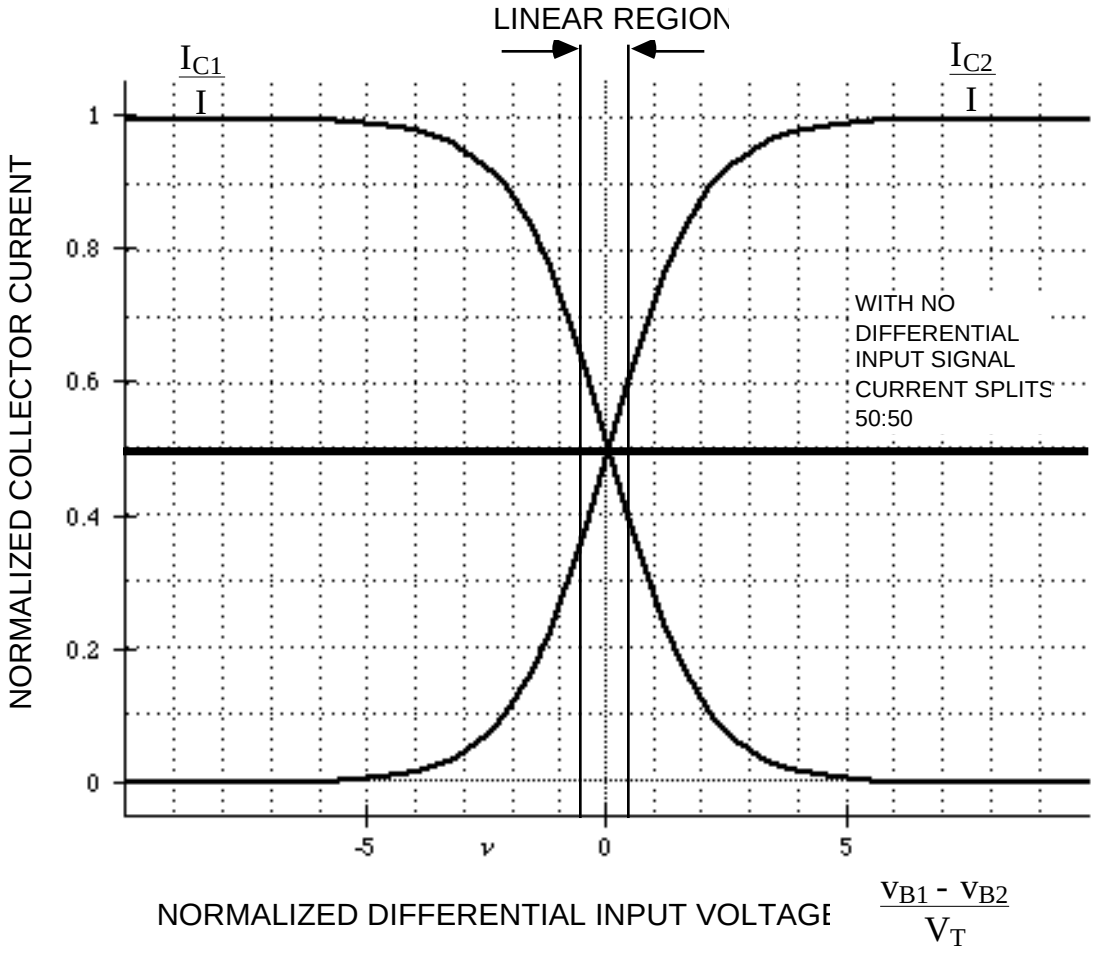
$$\frac{i_{E1}}{i_{E1} + i_{E2}} = \frac{1}{1 + e^{\frac{(v_{B2} - v_{B1})}{V_T}}} \qquad \text{and} \qquad \frac{i_{E2}}{i_{E1} + i_{E2}} = \frac{1}{1 + e^{\frac{(v_{B1} - v_{B2})}{V_T}}}$$

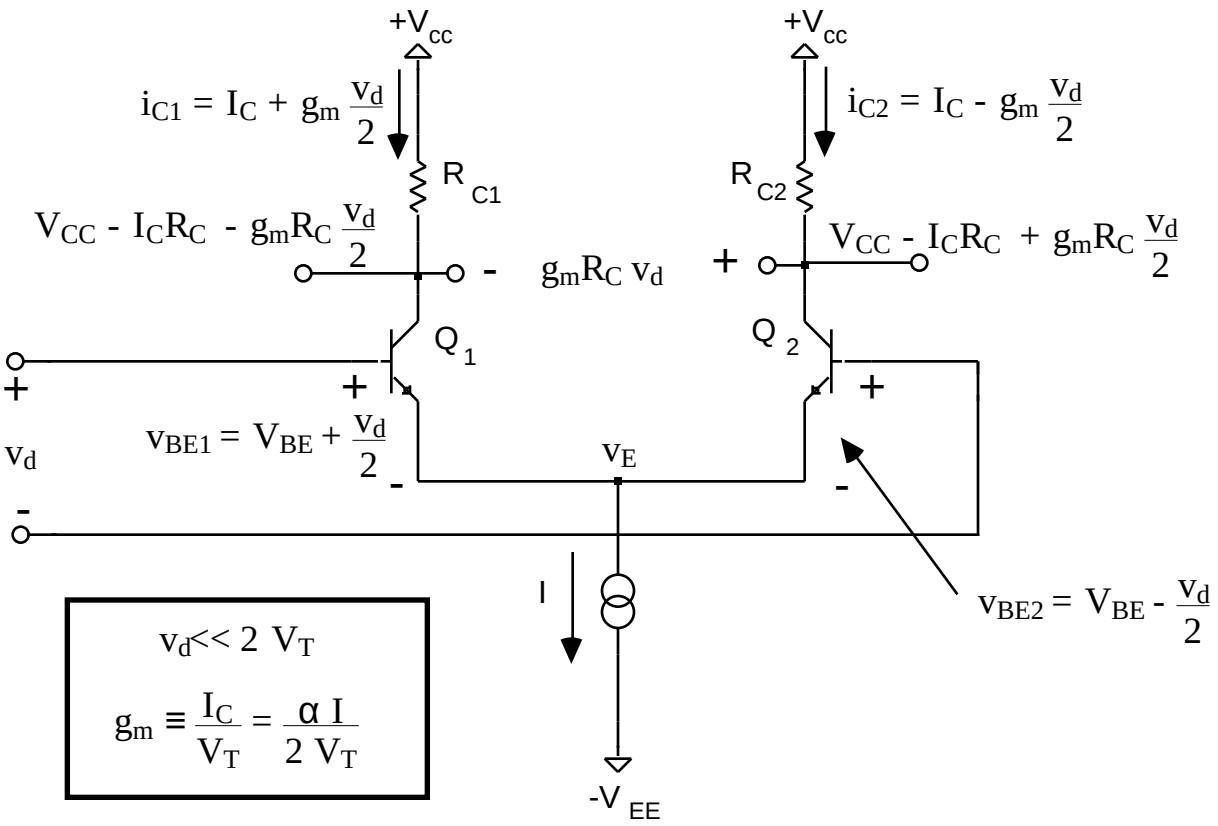
• Combined with the constraint imposed by the current source that they both sum to I,

$$i_{E1} + i_{E2} = I$$

$$i_{E1} = \frac{I}{1 + e^{\frac{(v_{B2} - v_{B1})}{V_T}}} \qquad \text{and} \qquad i_{E2} = \frac{I}{1 + e^{\frac{(v_{B1} - v_{B2})}{V_T}}}$$

• Which represent the currents as functions of the input voltage and shows that we have an extremely sensitive variation of the i_E's with the differential-mode input voltages.





• Redefining the steady-state current in each collector as,

$$I_C = \frac{\alpha I}{2}$$

• We see that the collector currents can be expressed in a form that looks like a common emitter amplifier gain equation with v_{be} given by $v_d/2$,

$$i_{C1} = I_C + g_m \frac{v_d}{2} \qquad i_{C2} = I_C - g_m \frac{v_d}{2}$$

• And the output voltages (considering both DC and AC components) are,

$$v_{C1} = \underbrace{(V_{CC} - I_C R_C)}_{\text{quiescent}} \underbrace{- g_m R_C \frac{v_d}{2}}_{\text{signal}} \qquad v_{C2} = \underbrace{(V_{CC} - I_C R_C)}_{\text{quiescent}} + \underbrace{g_m R_C \frac{v_d}{2}}_{\text{signal}}$$

• The **differential gain** (taken across the two outputs) is then,

$$A_d = \frac{v_{C1} - v_{C2}}{v_d} = - g_m R_C$$

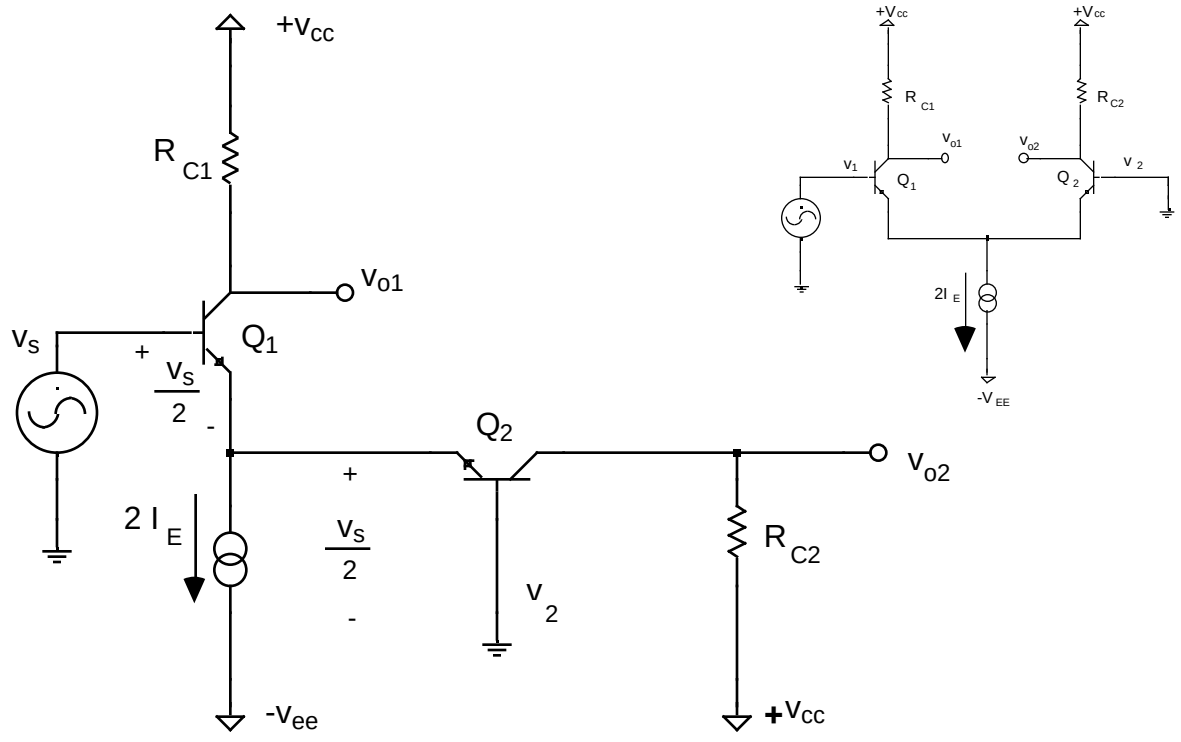
(written as for a CE amplifier)

(To reverse the sign, simply reverse your connections to the outputs!)

• And the **single-ended gain** (looking at only one of the two outputs is 1/2 of that....

$$A_d = \frac{v_{C1}}{v_d} = - \frac{1}{2} g_m R_C$$

• In order to understand the small-signal behavior of the differential pair, treat the circuit as a cascade of two single-transistor amplifiers, a CE and a CB (a CASCODE) and ask: WHAT IS THE GAIN?



• Start by grounding one of the inputs (to make it simpler to understand)...

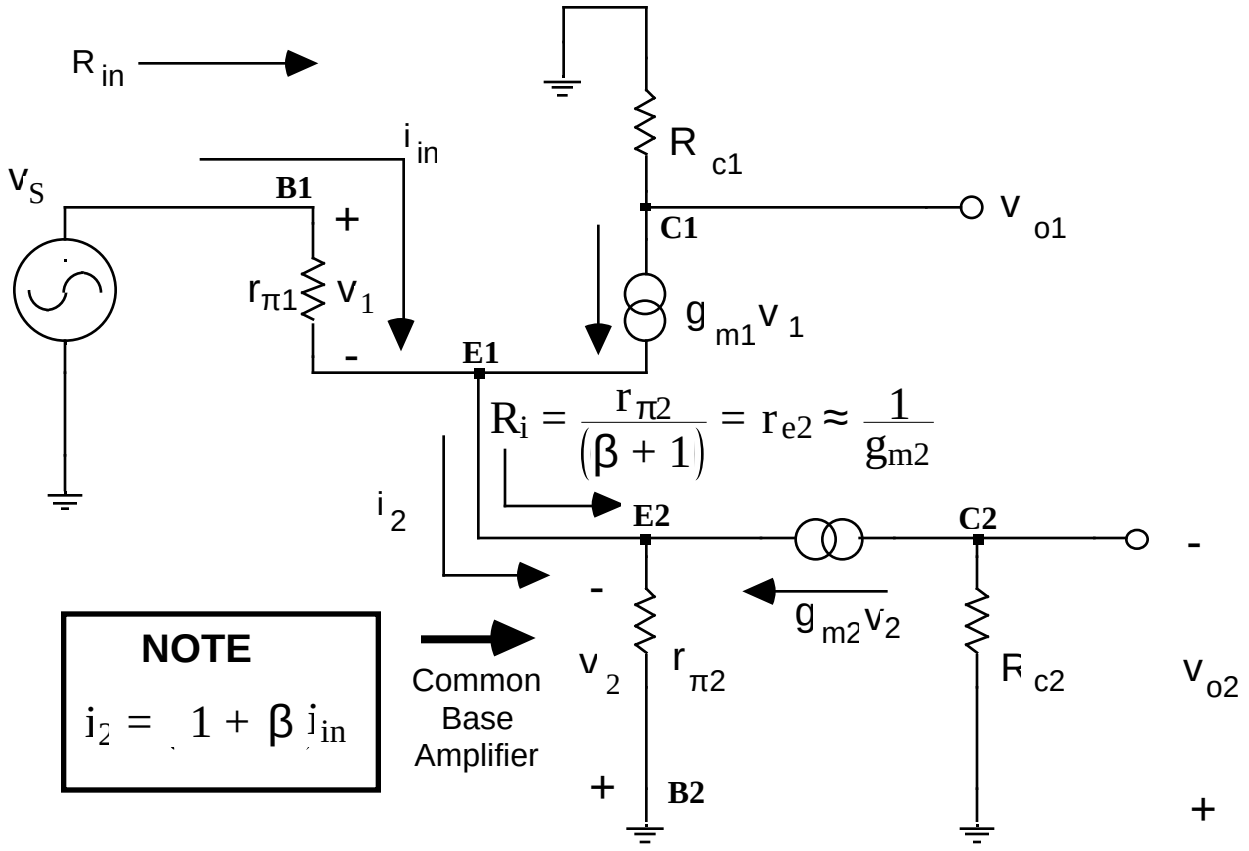
Note that, it looks like two different configurations, depending upon whether you are looking at v_{o1} or v_{o2} (**think about this for a minute!**)...

From the point of view of v_{o1}, it is a **common emitter amplifier that is degenerated** by the load on its emitter (Q2).

From the point of view of v_{o2}, it is a **common collector (emitter follower) amplifier with a common base amplifier as its load.**

(Remember: the $2I_E$ current source is only there for the DC circuit!)

• **MAKE A SMALL-SIGNAL EQUIVALENT CIRCUIT....**



(Here, let's use separate notation of the r_π's, g_m's, etc.... below we will assume they are the same.)

• First look at the **input resistance** of the amplifier...

• By inspection, looking into the base of Q_1, (Assuming r_π's are the same.)

$$R_{in} = r_\pi + (\beta + 1)\left(\frac{r_\pi}{\beta + 1}\right) = 2r_\pi$$

Scaling because you are looking into the base of Q1

Divide by (ß + 1) because you are looking into the emitter of Q2. This is also the same as r_e for Q2.

• So, the input resistance is **twice** what it would be for a common emitter amplifier with the same transistor.

• Now try to figure out the **gain**.... Start by computing the voltage at the input of the common base stage, v_2...

$$v_2 = -i_2 r_e = -\left(\frac{v_s}{R_{in}}\right)(\beta + 1)\left(\frac{r_\pi}{\beta + 1}\right) = -\frac{r_\pi}{2r_\pi} v_s = -\frac{v_s}{2}$$

The load of

This term is the current gain of Q1 from B to E

Minus sign because of the way we defined v (look at the schematic)...

This term is the input current to Q1

This term is just r_e

• Now we can calculate the output voltage v_{o2}

$$v_{o2} = -g_m v_2 R_c = -g_m\left(\frac{-v_s}{2}\right) R_c = g_m R_c\left(\frac{v_s}{2}\right)$$ Interesting Result!

• From this we can find the gain...

$$A_{v2} = \frac{v_{o2}}{v_s} = \frac{g_m R_c}{2}$$

• This is **1/2 the gain of a comparable common base amplifier**....

• Also note that the other output (v_{o1}) is an inverting version of (v_{o2}) :

$$v_1 = \frac{v_s}{2} \qquad v_{o1} = -g_m \frac{v_s}{2} R_c \qquad A_{v1} = \frac{v_{o1}}{v_s} = -\frac{g_m R_c}{2}$$

Hopefully you can see why this is the case!

• Note that you can obtain the same result using r_π' and g_m' for an un-bypassed emitter resistance of $R_E = r_e = 1/g_m$.

• So, at this point we know that:

- the input resistance is $2r_\pi$
- the gain is $\frac{g_m R_c}{2}$

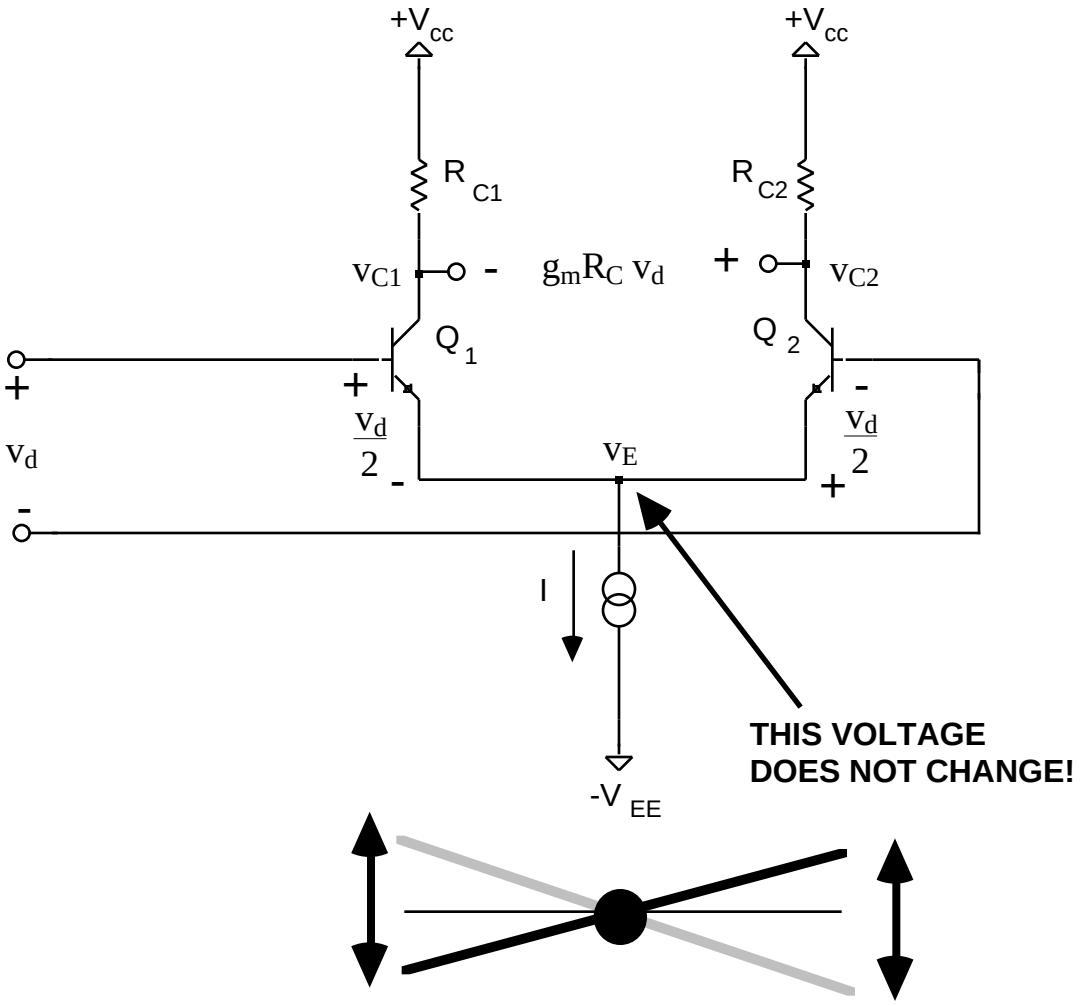
(or -1 times that, depending on which output you use) **-> this is 1/2 the gain of a comparable common-emitter amplifier.**

• This circuit can be used as a symmetrical “phase-splitter” to get two equal amplitude versions of a signal 180° out of phase with each other

5: HALF-CIRCUIT MODEL OF DIFFERENTIAL PAIR

• The half-circuit model is a way of taking advantage of the symmetry of the differential pair circuit to simplify analysis **in settings where we either drive the inputs differentially (and symetrically) or we drive them in common-mode**. The half-circuit model *does not work for asymmetrically driven differential pairs* (i.e. one input grounded, the other driven).

• In this example, we **drive the circuit differentially** (when one output swings up, the other swings down)... this is not the same as the previous case where we studied the frequency response because then we grounded one input!

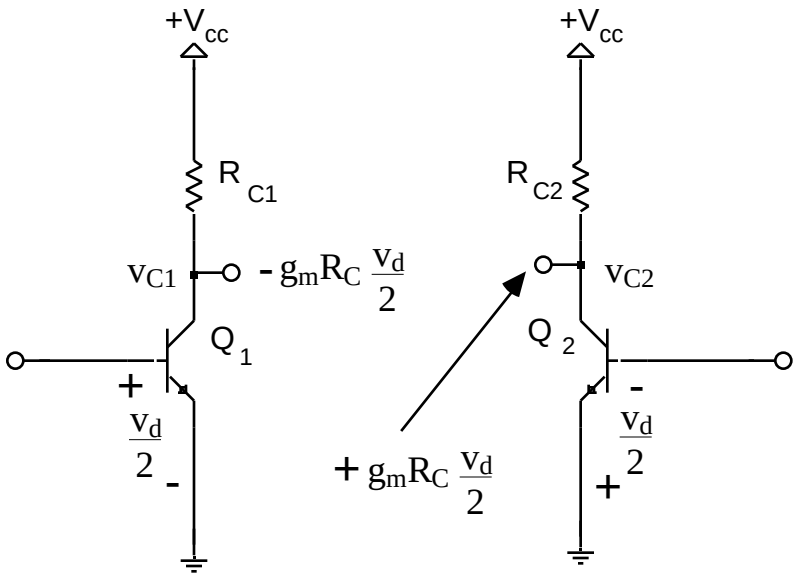


• The idea there is that the voltages pivot about the common point between the emitters (the current source)

-> v_E does not change

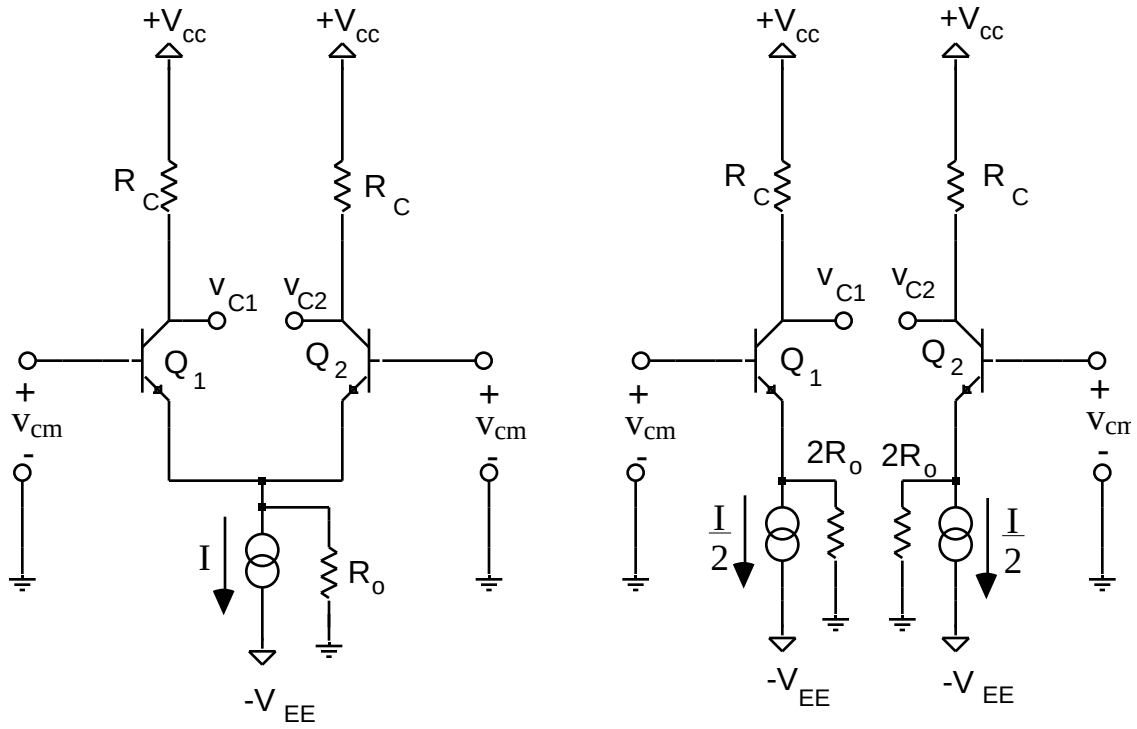
-> can thus treat v_E as a power supply, so it is a ***virtual ground*** for small signals...

• Just **split the differential pair** in half (it looks like two identical common-emitter circuits)...



• The half-circuit idea *works for any connections between the two sides*. For example, if there were a resistor of value R connected between the collectors, you could split it into two resistors of value R/2, each connected with one end to one of the collectors and the other end to ground.

6: HALF-CIRCUIT MODEL AND COMMON-MODE OPERATION



(Note that R_o can be shown connected to ground, depending upon the current source.)

• Use the half-circuit concept from above to analyze common-mode operation (which preserves the symmetry that allows the half-circuit model to be used in the first place).

• Relationship of half-circuit to common-mode circuit: the two halves are identical so the potential at the emitters is the same. *Circuit theory says we can connect together two nodes that have the identical voltages without affecting the operation of the circuit* -> connecting the emitters in the half-circuit leads to the physical equivalent of the circuit on the left.

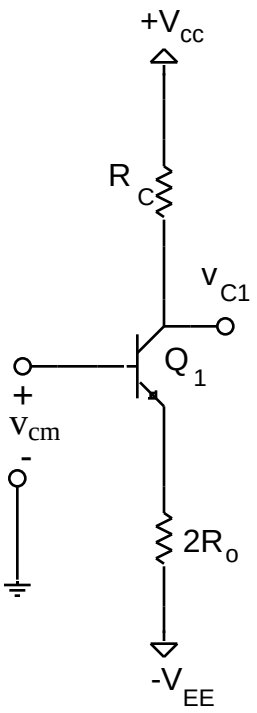
• This time, assume a current source with a shunt resistance R_o... (REMEMBER the output resistance, R_o, of the "realistic" current sources we looked at before...)

• Each of the independent current sources provides a current of $\frac{I}{2}$ and has an equivalent shunt resistance of $2R_o$...

• Both inputs are driven by the same signal (otherwise it wouldn't be common mode!)...

• IDEALLY common mode signals would be rejected! What happens here?

• With the non-ideal current source, the voltage and the current at the V_E node changes with the input signal.



This is the half-circuit for AC signals....

(This method is easier to understand than Sedra & Smith's.)

• Note that the current source is not shown because this is an AC circuit, but you would still re-draw it to obtain a small-signal circuit!.

• This is just an **emitter degenerated common emitter amplifier!** So, just write down the equation from memory (yeah, sure...),

$$v_{c1} = - g_m' R_C v_{be} = - \frac{g_m}{1 + g_m 2R_o} R_C v_{cm}$$

• If $g_m 2R_o >> 1$, we can make the approximation,

$$v_{c1} = - \frac{R_C}{2R_o} v_{cm}$$ and, by symmetry, also know that, $$v_{c2} = - \frac{R_C}{2R_o} v_{cm}$$

• This gives a (single-ended output) gain of,

$$A_{cm} \approx - \frac{R_C}{2R_o}$$

• For R_C of 5 kΩ and R_o of 250 kΩ, this gives,

$$A_{cm} \approx -\frac{R_C}{2R_o} = -\frac{1}{100}$$ (-40dB, taking the absolute value, of course)

• This is ***attenuation***, which is exactly what you want for common mode signals (which are often noise that you do not want to amplify)!

7: COMMON-MODE REJECTION RATIO

• This parameter is used to express how well a differential amplifier can reject common-mode signals compared to how well it can amplify differential-mode signals.

$$\text{CMRR} \equiv 20 \log \left| \frac{\text{Differential Gain}}{\text{Common-Mode Gain}} \right| = 20 \log \left| \frac{A_d}{A_{cm}} \right| \text{ dB}$$

(CMRR is almost always expressed in dB...)

• **KEY POINT! If the output voltage is taken differentially, the common-mode gain will be zero since both outputs do exactly the same thing** (unless there are mismatches in transistors and/or resistors)!

• If the output is taken in a single-ended fashion, one can compute the CMRR...

• The single-ended output, differential gain (from before) is,

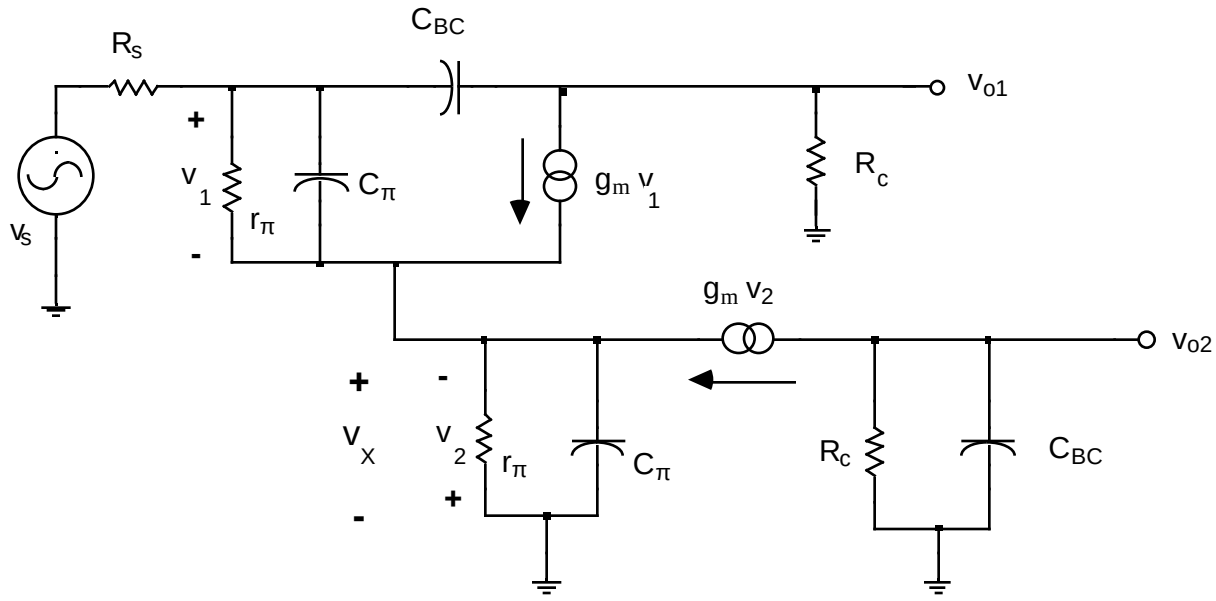
$$A_d = -\frac{1}{2} g_m R_C$$

• Therefore, the CMRR can be written as,

$$\text{CMRR} = 20 \log \left| \frac{-\frac{1}{2} g_m R_C}{-\frac{R_C}{2R_o}} \right| = 20 \log \left| g_m R_o \right| \text{ dB}$$

• It should be clear from the above equation that improving CMRR can be done via increasing g_m and/or R_o.

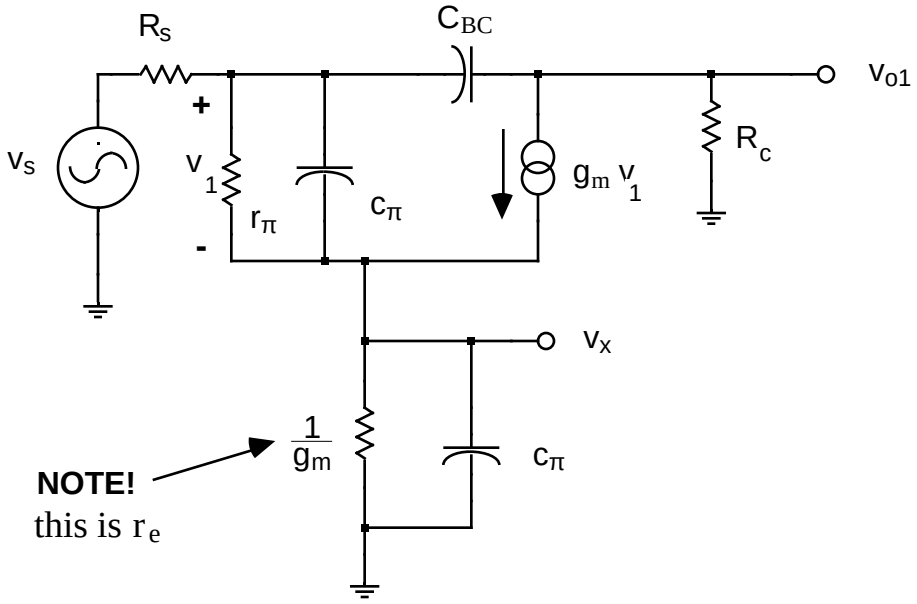
8: FREQUENCY RESPONSE OF THE DIFFERENTIAL AMPLIFIER



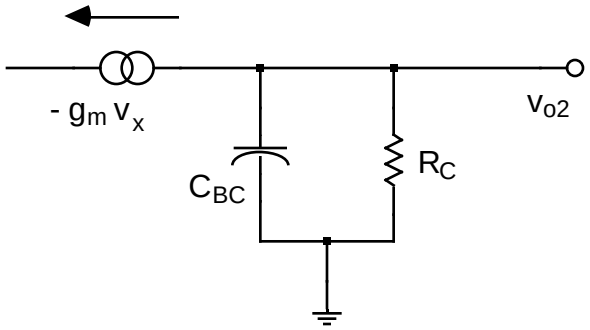
• For this analysis, add R_s, neglect r_o and r_X and assume that both transistors and their bias conditions are the same.

Break this into <u>two</u> problems:

<u>Part I</u> going from the input signal v_s to output V_{o1}



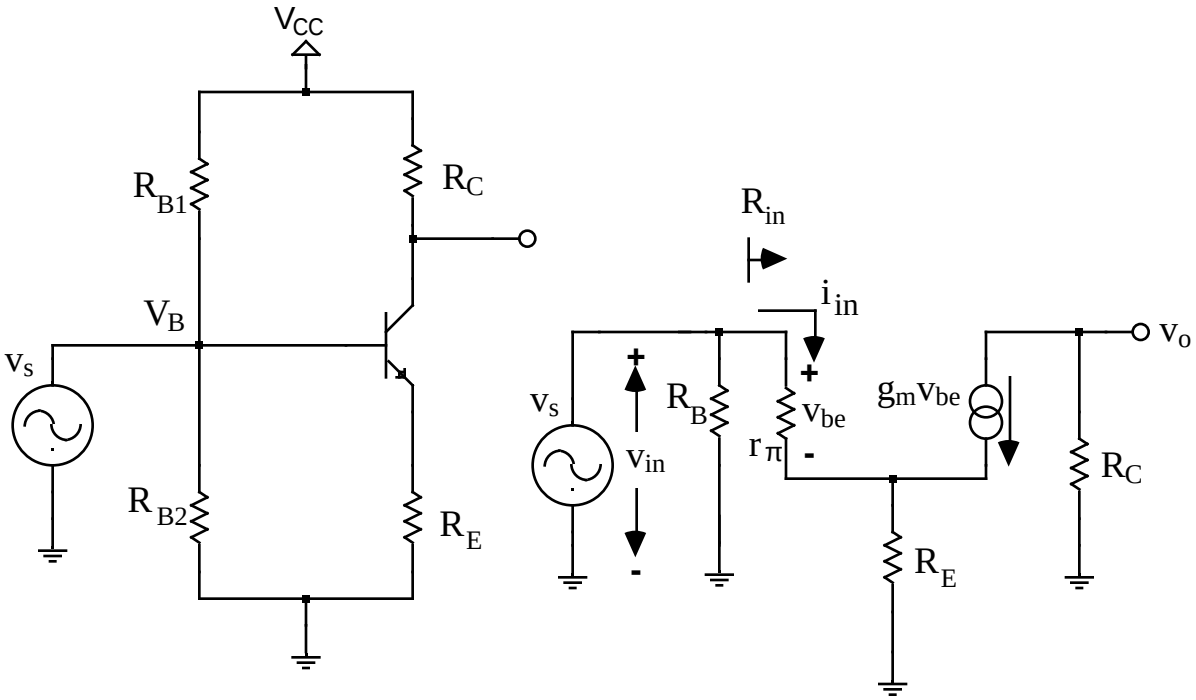
Part II going from the intermediate signal v_x to output V_{o2}



• This makes the analysis much easier to follow!

BEFORE LOOKING AT PART I...

• Remember about **incorporating an emitter resistance into a "new" small signal model for the transistor**? This was the principle of local feedback that led to decreased gain for emitter degenerated common emitter amplifiers.



• Thus, you have effectively replaced the original hybrid-π model with a new one with an INCREASED r_π (now called r_π') and a DECREASED g_m (now called g_m')....

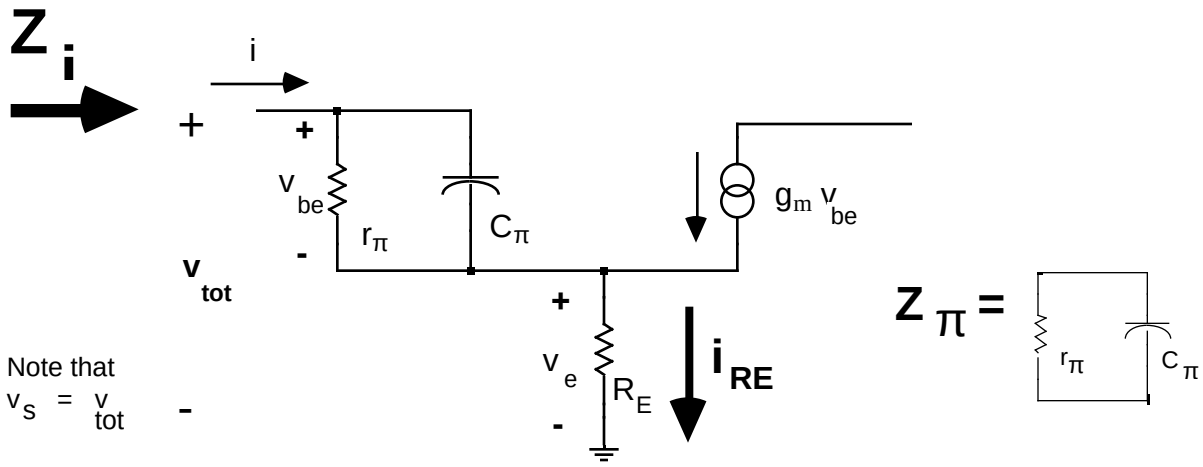
$$r'_\pi \equiv r_\pi\left(1 + g_m R_E\right)$$

$$g'_m \equiv \frac{g_m}{\left(1 + g_m R_E\right)}$$

• Now we will see that the same approach works if you have an ***IMPEDANCE*** in the emitter circuit instead of a resistance!

• We will see that we can also suitably "modify" C_π ! This is also the result of local feedback effects.

• Consider the same circuit we used in the common emitter lecture but with C_π taken into consideration...



• The approach is to consider the current and voltage at R_E and the total voltage and current into the base circuit (as shown above) and then to try to write a new expression that gives the correct total voltage and current for a "new" parallel RC combination at the base circuit....

• In other words, we want to modify the base circuit to take into account R_E so we can "ground" the emitter and treat it like a common-emitter amplifier after that.

• The impedance in the base circuit is,

$$z_\pi = r_\pi \| \frac{1}{sC_\pi} = \frac{r_\pi}{1 + sC_\pi r_\pi} = \frac{1}{y_\pi}$$

• And the current flowing in the emitter resistance R_E is,

$$i_{R_E} = \left(y_\pi + g_m\right) v_{be}$$

• And the voltage across R_E is,

$$v_e = R_E \left(y_\pi + g_m\right) v_{be}$$

• Now write an expression for the total input voltage,

$$v_{tot} = v_{be} + \underbrace{R_E \left(y_\pi + g_m\right) v_{be}}_{v'_e}$$

• And the input current into the "new" base-circuit impedance z_π is,

$$i = \frac{v_{be}}{z_\pi}$$

• Now (finally!) we can write an expression for the **TOTAL input impedance** considering both the input impedance of the base circuit plus the effects of the emitter circuit...

$$z_{in} = \frac{v_{tot}}{i} = \left(\frac{z_\pi}{v_{be}}\right)\left[v_{be} + R_E \left(y_\pi + g_m\right) v_{be}\right] = z_\pi + R_E + z_\pi R_E g_m$$

$$= R_E + z_\pi \left(1 + g_m R_E\right)$$

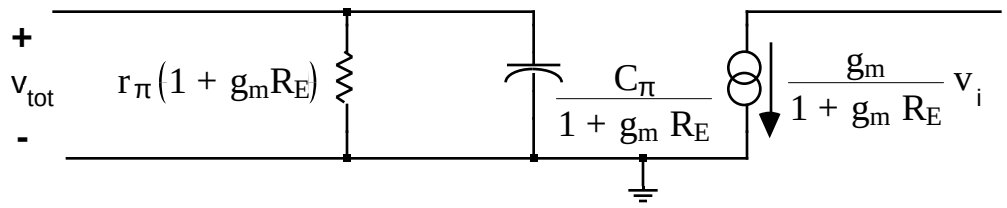
• Substitute for z_π....

$$= R_E + \frac{r_\pi \left(1 + g_m R_E\right)}{1 + s C_\pi r_\pi}$$

• At last... PAY DIRT!! It looks like a parallel RC combination in series with R_E!

$$z_{in} = R_E + r_\pi \left(1 + g_m R_E\right) \| \frac{1}{S\left(\frac{C_\pi}{1 + g_m R_E}\right)}$$

• Our “new” equivalent circuit (neglecting R_E)....

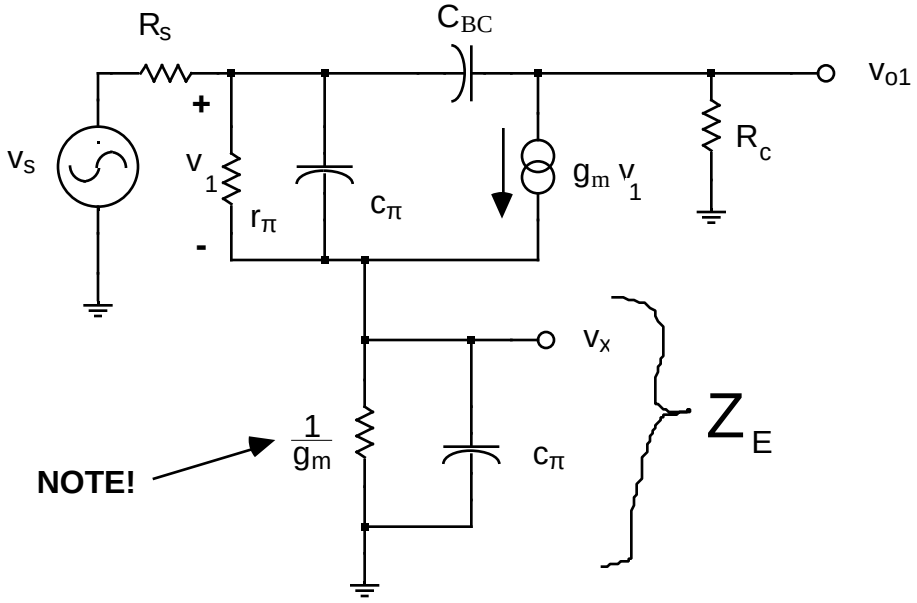


• **NOTE**: here we have neglected R_E because it is $1/g_{m2}$ when the load is a CB stage, as it is here.... if you put it into the above schematic, it makes things a bit less clear (but more accurate!). You can look at the "full" derivation in Gray and Meyer, "Analysis and Design of Analog Integrated Circuits," on pages 491 - 498.

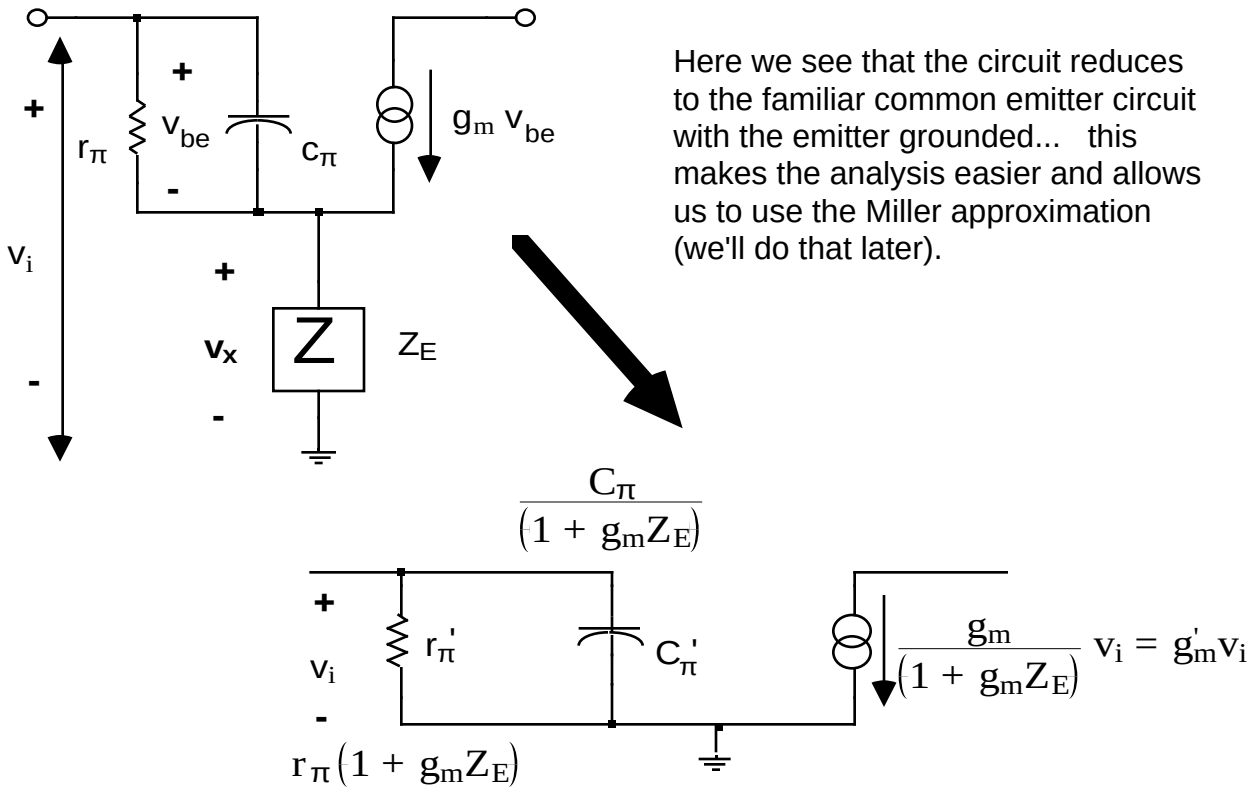
• **Note** that for a differential pair, taking $R_E = r_e$ into account yields $r_\pi' = 2r_\pi$, $C_\pi' = C_\pi/2$ and $g_m' = g_m/2$.

NOW FOR PART I...

• It looks just like the above, but with an emitter ***IMPEDANCE*** rather than just an emitter resistance....



• In order to get transfer functions (i.e. Both $\frac{v_{o1}}{v_s}$ and $\frac{v_x}{v_s}$) look at the results we just obtained.



Here we see that the circuit reduces to the familiar common emitter circuit with the emitter grounded... this makes the analysis easier and allows us to use the Miller approximation (we'll do that later).

• For PART I, we know that,

$$Z_E = \frac{\frac{1}{g_m} r_e}{1 + s \frac{c_\pi}{g_m}}$$ and thus our "scaling factor"....

$$(1 + g_m Z_E) = 2 \frac{\left(1 + s \frac{c_\pi}{2 g_m}\right)}{\left(1 + s \frac{c_\pi}{g_m}\right)}$$

(Note that $C_\pi/g_m = C_\pi r_e$... perhaps more intuitive as an RC time constant.)

• This means there is a zero at $w_{z1} = \frac{2 g_m}{c_\pi}$ and a pole at $w_{p1} = \frac{1}{2} w_{z1} = \frac{g_m}{c_\pi}$

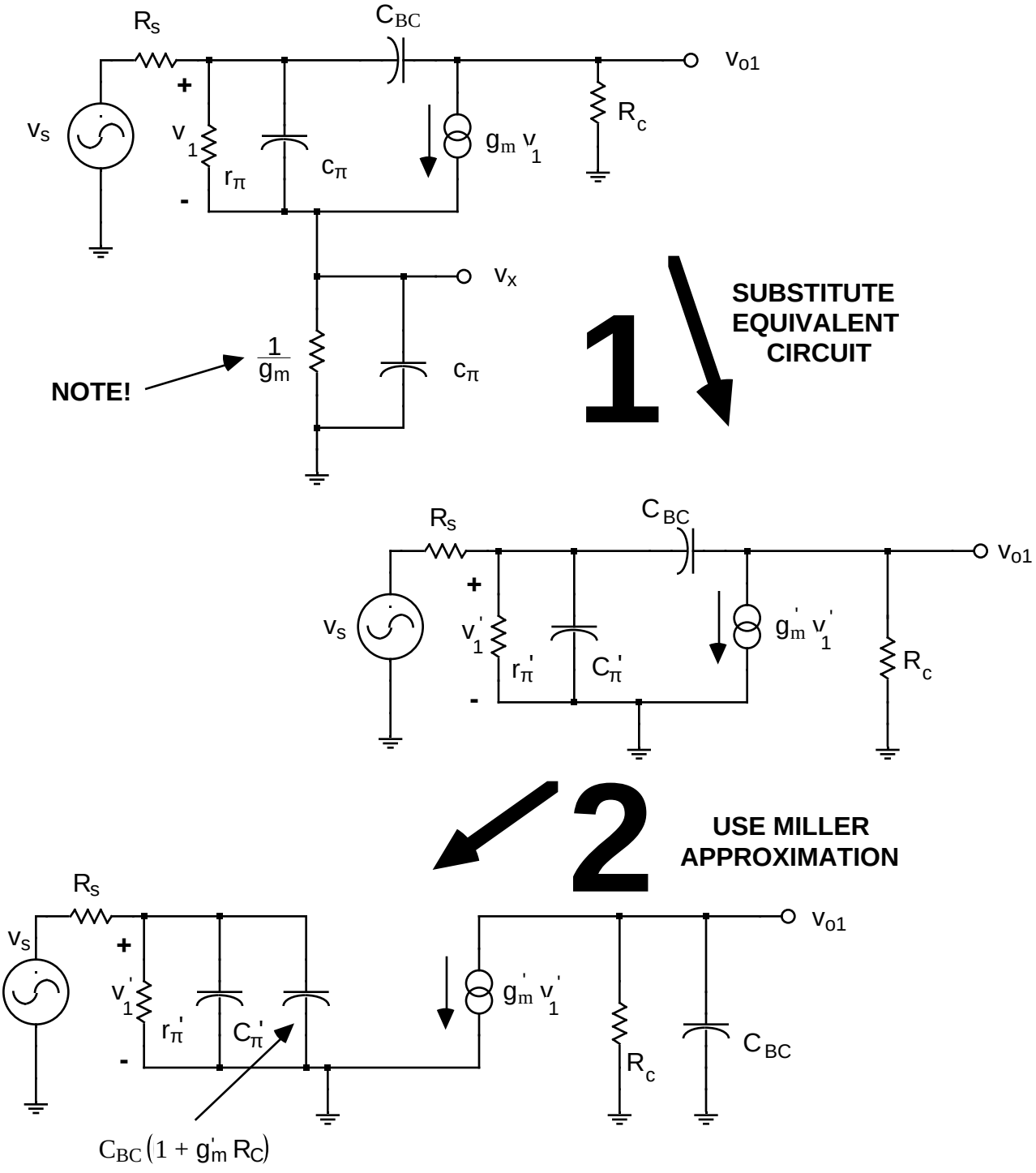
• Practically... **assuming the pole and zero cancel since they are so close in frequency**.... the “scaling factor” reduces to,

$$1 + g_m Z_E \approx 2$$

• Thus, we get an answer that looks a bit familiar (remember all those factors of two?).

$$r'_\pi \approx 2r_\pi \qquad c'_\pi \approx \frac{c_\pi}{2} \qquad g'_m \approx \frac{g_m}{2}$$

NOW, USING THESE NEW VALUES FOR THE "EQUIVALENT" TRANSISTOR, SOLVE PART 1....



NOTE THAT: $A_v' = - g_m' R_C$ so the Miller capacitance is $C_{BC}(1 + g_m' R_C)$

• The **input time constant** is given by,

$$\tau_{in} = \left(R_S \parallel r'_\pi\right)\left[c'_\pi + C_{BC}\left(1 + g'_m R_C\right)\right] = \left(R_S \parallel 2r_\pi\right)\left[\frac{c_\pi}{2} + C_{BC}\left(1 + \frac{g_m}{2} R_C\right)\right]$$

• **NOTE that if $R_s = 0$, r_x is the main thing that sets the upper cutoff frequency....**
The above equation (approximate!) considering r_x and r_o is:

$$\tau_{in} = \left(\left[R_S + r_x\right] \parallel 2r_\pi\right)\left[\frac{c_\pi}{2} + C_{BC}\left(1 + \frac{g_m}{2}\left[R_C \parallel r_o\right]\right)\right]$$

• The **output circuit time constant** is,

$$\tau_{out} = C_{BC} R_C$$

• And we can now write the overall transfer function equation for the $\frac{v_{o1}}{v_s}$ path.....

$$\frac{v_{o1}}{v_s} = T(S) = -\left(\frac{r'_\pi}{R_S + r'_\pi}\right) g'_m R_C \left(\frac{1}{1 + S\tau_{in}}\right)\left(\frac{1}{1 + S\tau_{out}}\right)$$

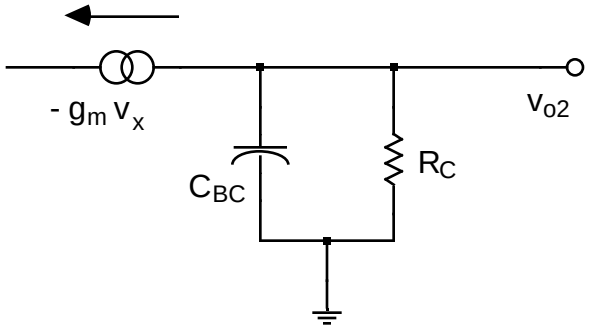
DC AC

• Substituting in for the “primes”....

$$\frac{v_{o1}}{v_s} = T(S) = -\left(\frac{2r_\pi}{R_S + 2r_\pi}\right) \frac{g_m}{2} R_C \left(\frac{1}{1 + S\tau_{in}}\right)\left(\frac{1}{1 + S\tau_{out}}\right)$$

This is a low-pass response only (no high-pass)... this is a DC-coupled amplifier!

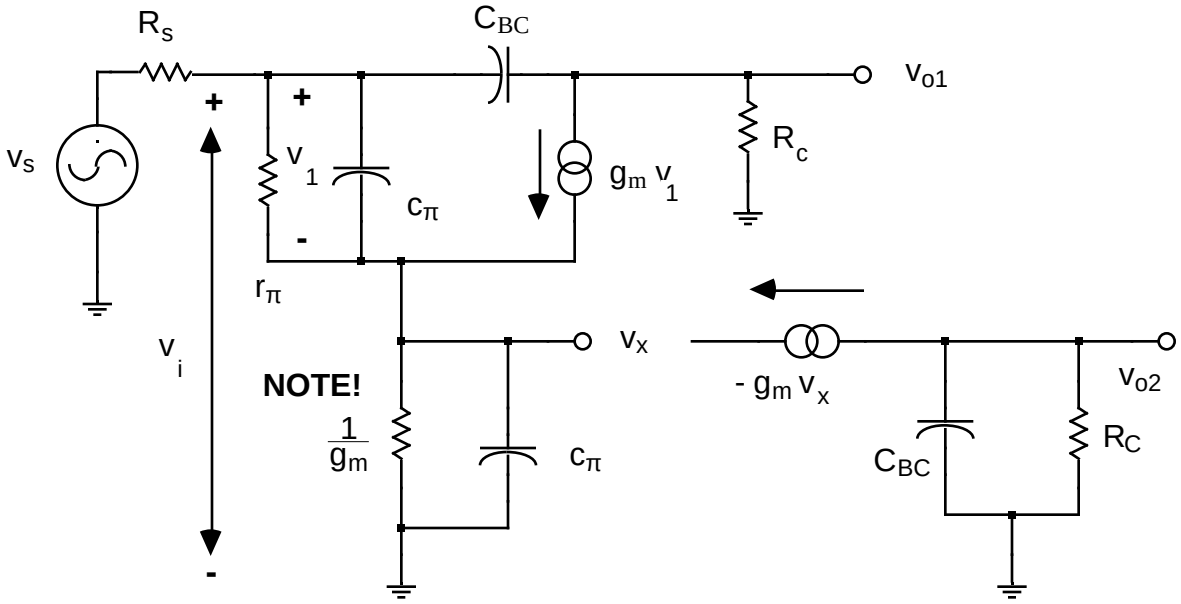
NOW DO PART II...



• Assuming (see above) that,

$v_x = \frac{v_i}{2}$ (where v_i is the voltage input to the base of Q_1, AFTER R_s...)

• We look at the schematic from PART I again....



• Knowing (from above) that the roll-off of the voltage v_i is given by,

$$\frac{1}{1 + S\,\tau_{in}}$$

• v_i can be found as a function of v_S by simple voltage division, knowing that the input resistance (after R_S) is $2r_\pi$

$$v_i = \left(\frac{2\,r_\pi}{R_S + 2\,r_\pi}\right) v_S \left(\frac{1}{1 + S\,\tau_{in}}\right)$$

input voltage divider term

roll-off due to input circuit

• Again, we use the fact that v_X is simply 1/2 of v_i....

• We can also see that the output signal v_{o2} is,

$$v_{o2} = g_m v_x \frac{R_C}{1 + S\,R_C C_{BC}} = g_m \frac{v_i}{2} \frac{R_C}{1 + S\,\tau_{out}}$$

• Now we can find the complete transfer function for v_{o2},

$$\frac{v_{o2}}{v_s} = T(S) = \left(\frac{2r_\pi}{R_S + 2r_\pi}\right) \frac{g_m}{2} R_C \left(\frac{1}{1 + S\tau_{in}}\right)\left(\frac{1}{1 + S\tau_{out}}\right) = -\frac{v_{o1}}{v_s}$$

• THIS IS THE SAME AS FOR v_{o1}, but it is 180° out of phase....

9: SUMMARY OF DIFFERENTIAL PAIR SMALL-SIGNAL OPERATION

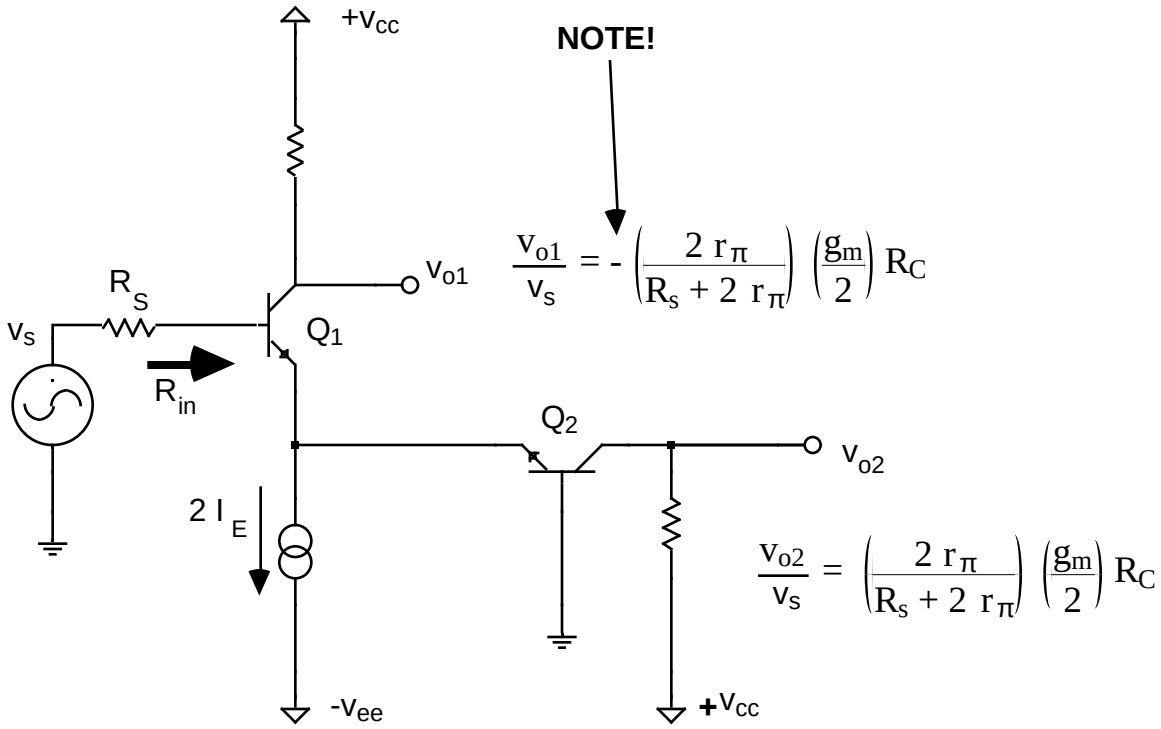
• $R_{in} = 2r_\pi$

• Both signal paths have a midband gain of $\frac{g_m}{2} R_C$ with an input voltage divider of $\frac{R_{in}}{R_S + R_{in}}$

• One path is inverting and the other one is non-inverting.

• Both paths have the **same time constants**!

• Small signal gain:



10: OTHER IMPERFECTIONS OF "REALISTIC" DIFFERENTIAL AMPLIFIERS

• This section deals with imperfections of differential amplifiers beyond just the common-mode issues considered thus far.

THESE ARE SOME KEY TERMS TO KNOW!

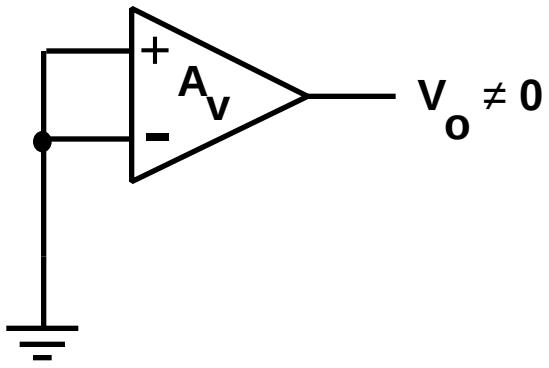
10.1 INPUT OFFSET VOLTAGE

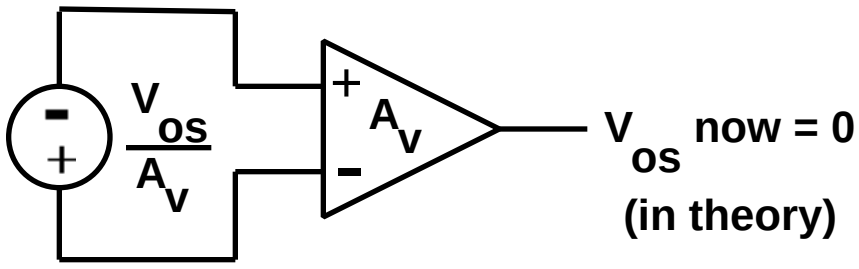
• If you ground both inputs of the differential pair, the output (taken differentially) should be zero, right? Well, in practice, it may not be....

• The input offset voltage is defined as the DC voltage that appears at the output with the inputs grounded, divided by the gain of the amplifier (to refer the offset to the input of the amplifier...).

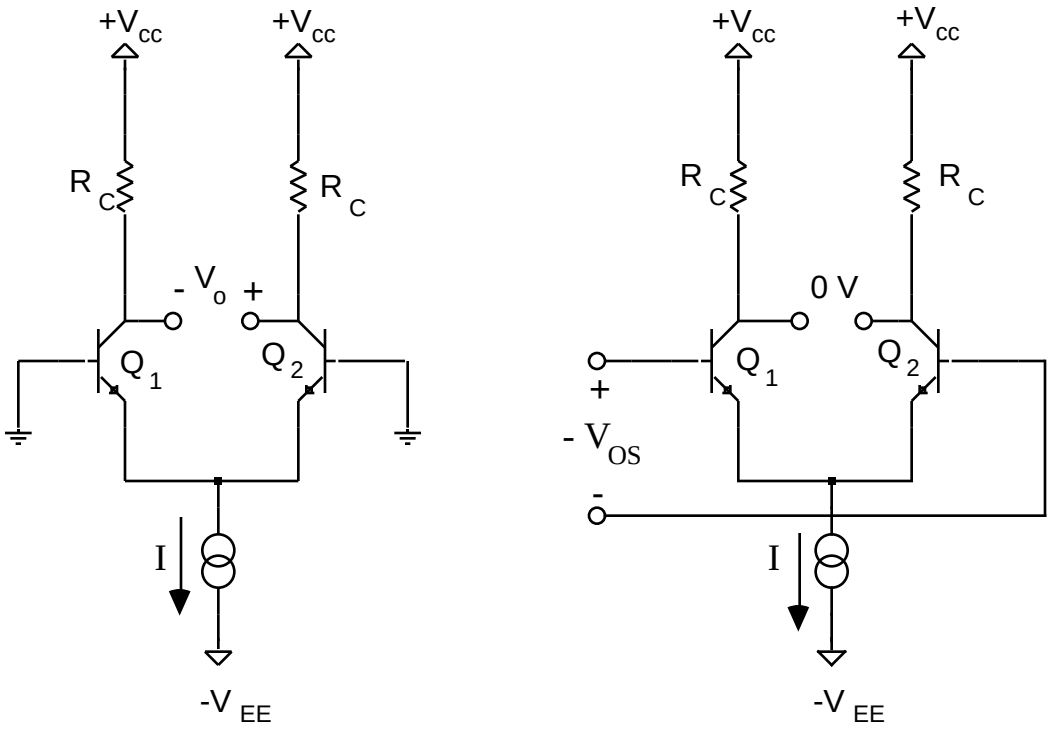
$$V_{OS} \equiv \frac{\text{Output voltage with inputs grounded}}{\text{Differential Gain}} = \frac{V_O}{A_d}$$

• If you apply a voltage $-V_{os}$ to the inputs of the amplifier, the output goes to zero (in theory) !!!!





• In other words, with an imperfect amp, you get V_o out if you ground the inputs... V_o is what you would get if you put V_{os} into a perfect amp with no offset!



• Where could this be a problem? If you cascade several DC-coupled amplifiers, the offset voltages get multiplied by the gains and eventually saturate the amplifier!

• Where does the offset come from?

• Mismatches in R_C's, mismatches in the transistors, etc....

• Consider offsets in the R_C's... (assume matched transistors)

• If the mismatch is evenly distributed between the two resistors (this is not as weird as it sounds, since you simply "split the difference" between the resistors and call the average value R_C...)

$$R_{C1} = R_C + \frac{\Delta R_C}{2} \qquad R_{C2} = R_C - \frac{\Delta R_C}{2}$$

• If the transistors are matched, the current will divide equally between them, allowing us to write,

$$V_{C1} = V_{CC} - \left(\frac{\alpha I}{2}\right)\left(R_C + \frac{\Delta R_C}{2}\right) \qquad V_{C2} = V_{CC} - \left(\frac{\alpha I}{2}\right)\left(R_C - \frac{\Delta R_C}{2}\right)$$

• Which gives an output voltage of,

$$V_O = V_{C1} - V_{C2} = \left(\frac{\alpha I}{2}\right)(\Delta R_C)$$

• To calculate the input offset voltage, we need to recall that A_d is given by,

$$A_d = g_m R_C \qquad \text{where} \qquad g_m = \frac{I_C}{V_T} = \frac{\frac{\alpha I}{2}}{V_T}$$

(note that this is not $\frac{g_m}{2} R_C$ because the output is taken differentially)

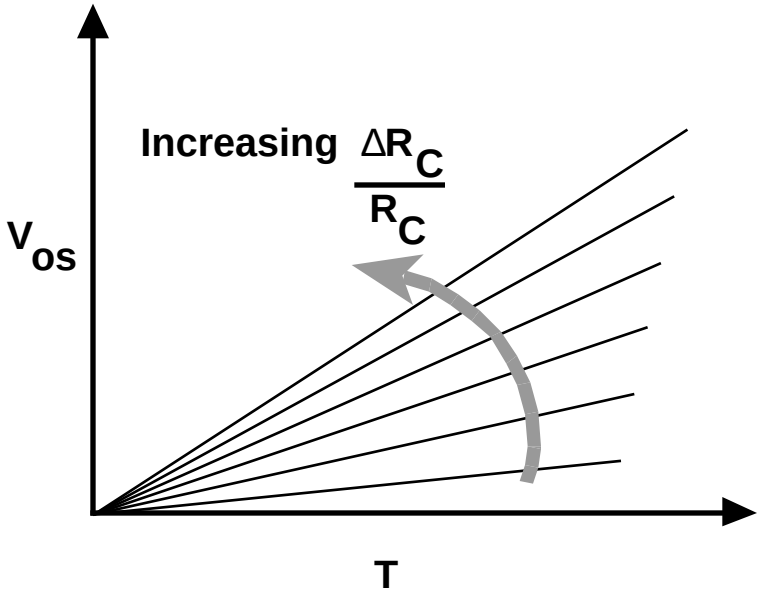
• Therefore, the input offset voltage is a function of the ***matching*** of collector resistors, not their absolute value,

$$|V_{OS}| = \frac{V_O}{A_d} = \frac{\left(\frac{\alpha I}{2}\right)(\Delta R_C)}{\frac{\left(\frac{\alpha I}{2}\right)}{V_T} R_C} = V_T\left(\frac{\Delta R_C}{R_C}\right)$$

Units of % change

≈ 26 millivolts

• Thus the offset is clearly a function of temperature $\left(V_T = \frac{kT}{q}\right)$ and the matching of the resistors,



• For +/- 1% resistors, this gives a maximum mismatch of 2% and maximum V_{OS} of 0.5 mV.

• You can do the same type of analysis for differences in the transistor parameters (Sedra and Smith consider differences in the emitter-base junction areas that in turn cause differences in I_S between the two devices).

• If you work out the same thing for this case, you end up with a similar-looking equation that gives V_{OS} in terms of I_S mismatch,

$$|V_{OS}| = \frac{V_O}{A_d} = V_T\left(\frac{\Delta I_S}{I_S}\right)$$

• Note that I_S is also a function of T... $I_S \quad T^{\alpha}$

10.2 INPUT BIAS AND OFFSET CURRENTS

• Input bias currents represent the currents required to turn on the input transistors (i.e. the BASE CURRENTS!!!).

• The input bias current is given by,

$$I_{B1} = I_{B2} = \frac{\left(\frac{I}{2}\right)}{\beta + 1}$$

the emitter current in each of the two transistors

• If the β's are mismatched, the input bias currents will also be mismatched!

• The **INPUT OFFSET CURRENT** is simply defined as the difference between them!

$$I_{OS} = |I_{B1} - I_{B2}|$$

• Using similar math as for the offset voltage, and assuming β mismatch given by,

$$\beta_1 = \beta + \frac{\Delta\beta}{2} \qquad \beta_2 = \beta - \frac{\Delta\beta}{2}$$

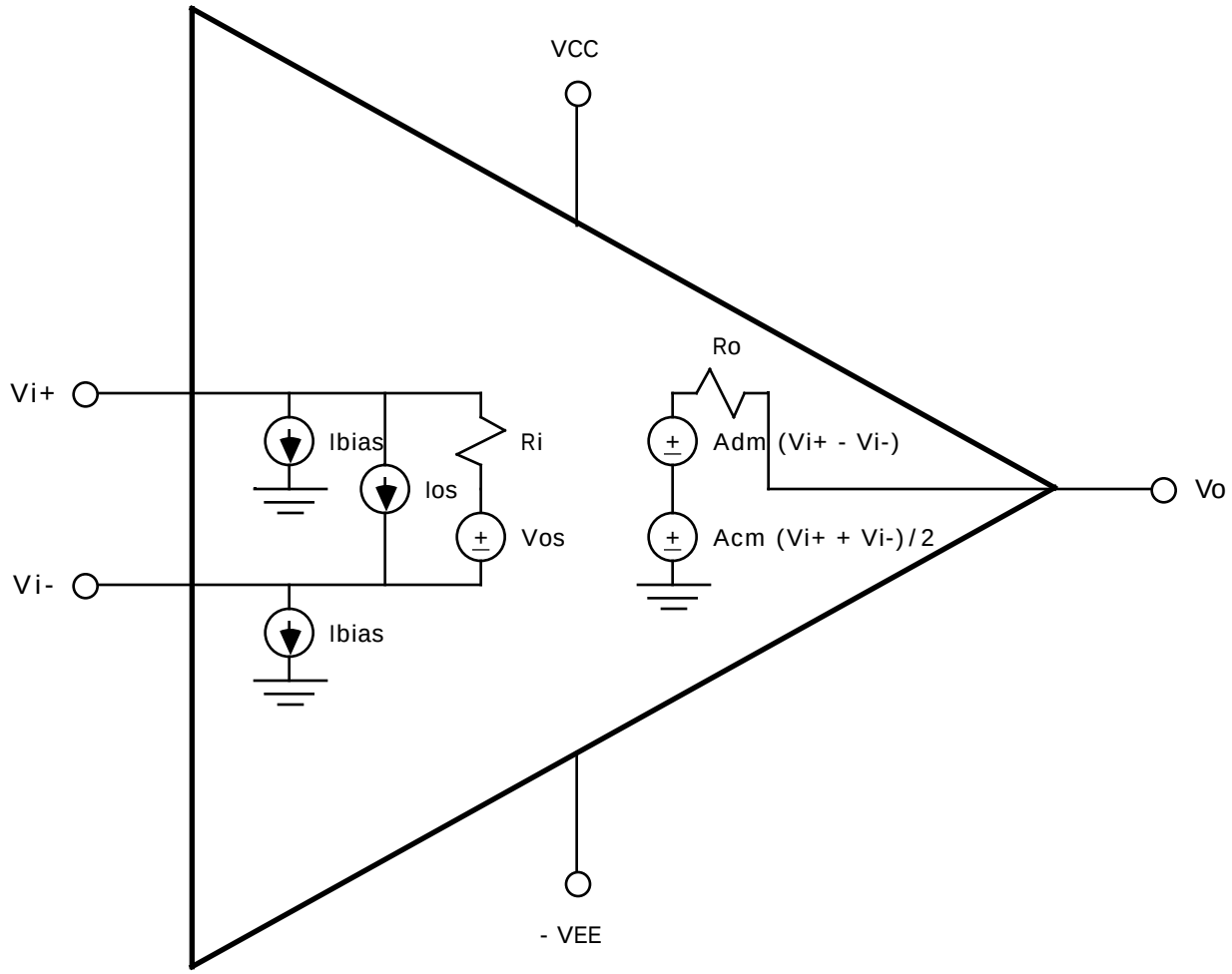
• It can be shown that (see Sedra and Smith),

$$I_{OS} = I_B\left(\frac{\Delta\beta}{\beta}\right)$$

where I_B is the "average" base current $\quad I_B = \frac{I_{B1} + I_{B2}}{2} = \frac{I}{2(\beta + 1)}$

• Here can improve things by reducing I_C (and hence I_B).

• Remember that the same terms apply to operational amplifiers, but may be brought about by more complicated effects (i.e. the same formulas may not always apply, but the basic principles do!).



Chapter 12: CURRENT SOURCES

Oh, you're supposed to pick up the OTHER end!!!
Berkeley EE student's thirty-second encounter with a soldering iron...

1: OBJECTIVES

• To consider:

The basics current source circuits.

The limitations of common current sources.

Design and use of current sources in multi-stage amplifiers.

• In order to build discrete amplifiers and integrated versions, current sources are necessary. In many cases, a single reference current must be scaled and "copied" (the term used is "mirrored") so that the bias points of several transistors on a chip are proportional to each other and the reference.

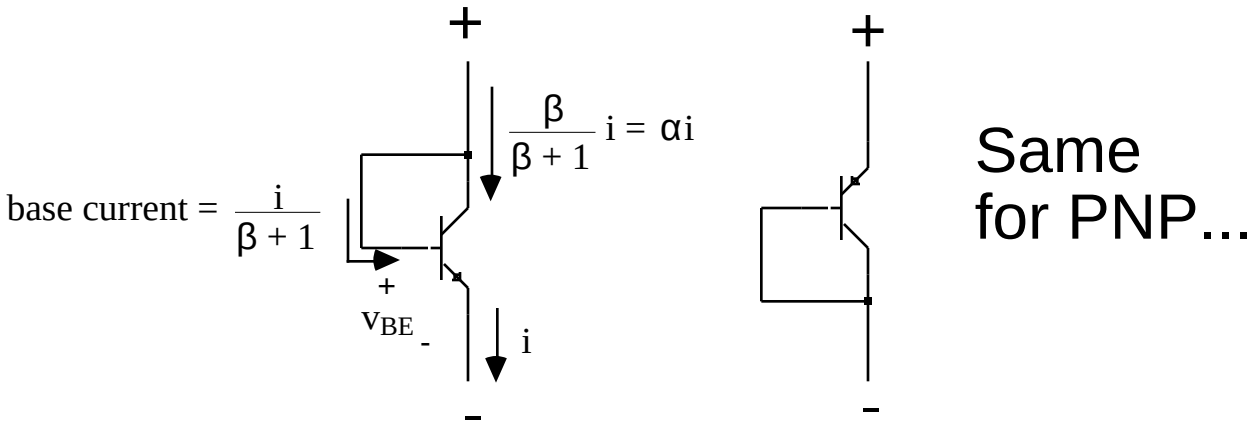
• The purpose of this chapter is to discuss such circuits and their uses.

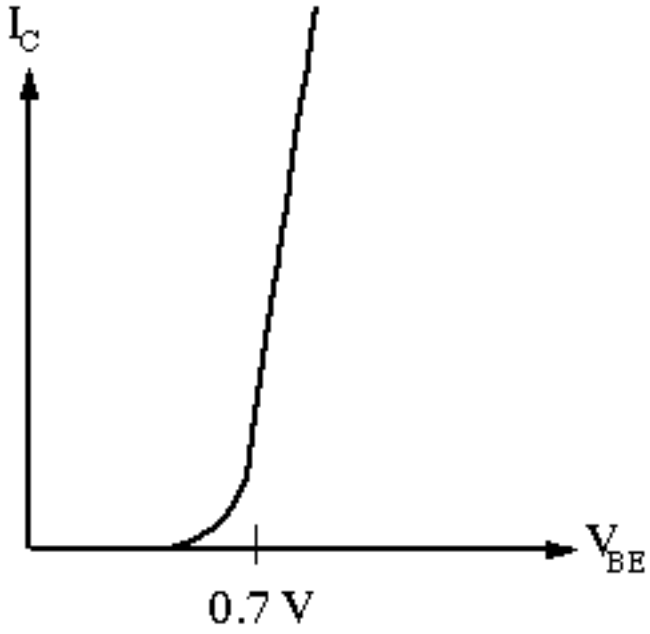
2: THE DIODE-CONNECTED TRANSISTOR

• This simple circuit is a building-block for current sources.

• A diode can be formed by connecting the base to the collector.

• The transistor now behaves like a diode with an I-V characteristic equal to the I_C - V_{BE} curve for the transistor. The resulting VBE can be applied to the base-emitter junction of a second transistor, which will have almost exactly the same collector current as the current flowing through the diode, making a "replica."

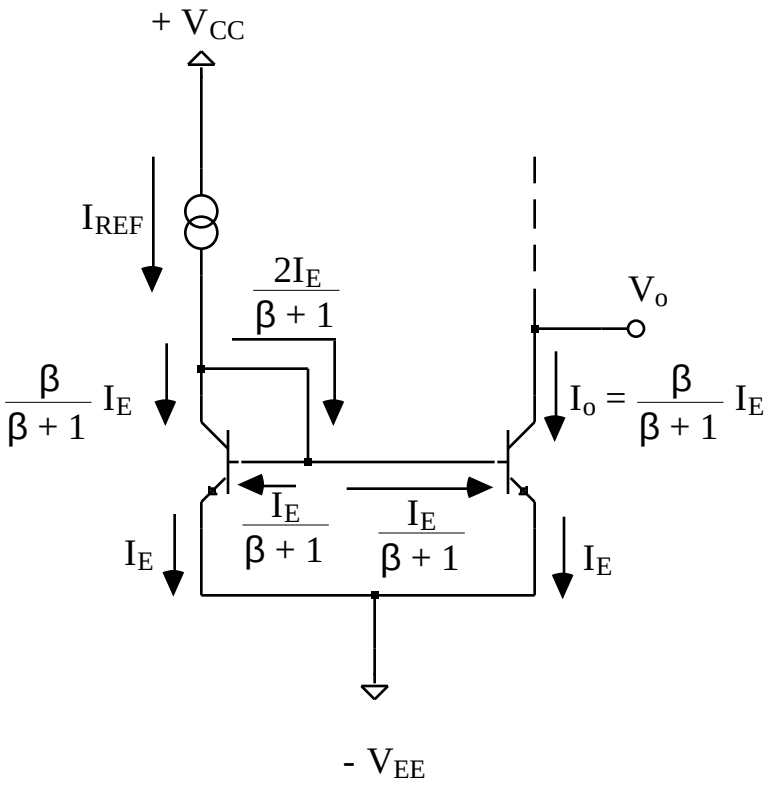




3: THE CURRENT MIRROR

• This circuit makes good use of the fact that the diode formed from a transistor has the same temperature coefficient as the transistor.

• Use one transistor as a v_{BE} reference -> feed in a desired reference current and the "diode" will establish the exact v_{BE} on the other transistor to get the same current to flow in it....



• Looking at the circuit above, it is obvious that,

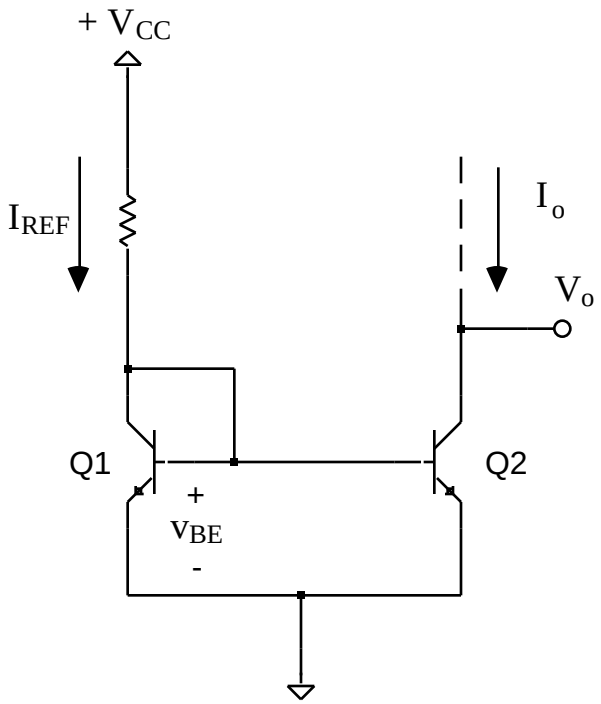
$$I_o = \frac{\beta}{\beta + 1} I_E$$

and therefore, we need (to get the desired I_0 out...),

$$I_{REF} = \frac{\beta}{\beta + 1} I_E + \frac{2I_E}{\beta + 1} = \frac{\beta + 2}{\beta + 1} I_E$$

• So, for large β, $I_{REF} = I_o$... For smaller β, need to make $I_{REF} > I_o$ by the correct amount...

4: A SIMPLE CURRENT SOURCE



$$I_{REF} = \frac{V_{CC} - V_{BE}}{R}$$

$-V_{EE}$ (or ground...)

V_{BE}'s are the same....

I_{C2} is the same as I_o

$$I_{REF} = \frac{V_{CC} - V_{BE}}{R} = I_{C1} + I_{B1} + I_{B2} = I_{C1} + \frac{I_{C1}}{\beta} + \frac{I_{C2}}{\beta} = I_{C1} + \frac{2I_{C1}}{\beta}$$

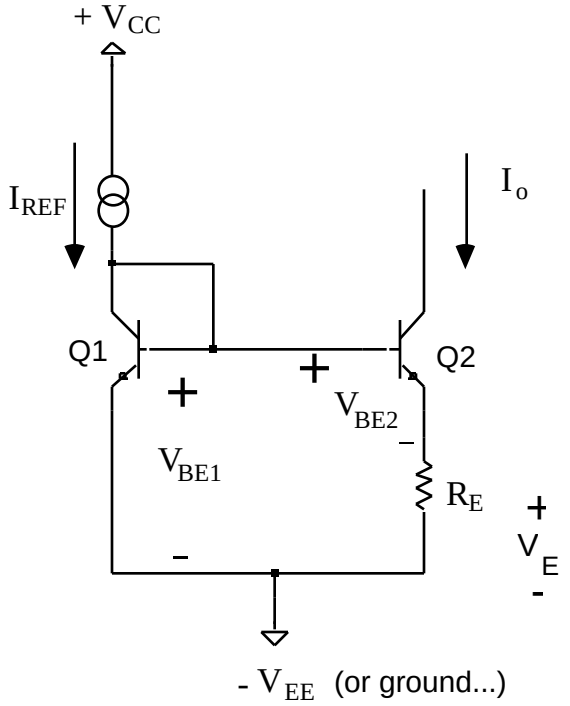
$$I_{C1} = I_{C2} = I_o$$

• As for the above case,

As $\beta \rightarrow \infty$ $I_o = I_{REF}$ (losing no current in the bases)

5: THE WIDLAR CURRENT SOURCE

You could get the reference current from a voltage reference and a resistor, for example...



• **Add in an emitter resistance in the output transistor....**

• As before, R_E stabilizes V_{BE2} against variations with Q_2's β, increases the output impedance (makes the current source more ideal... see below) and allows scaling of the current to any value less than I_{REF}.

• Looking at the circuit one can see (base currents are neglected for high β) that,

$$I_o = \frac{V_{BE1} - V_{BE2}}{R_E} = \frac{V_E}{R_E}$$

• The equation is not very useful in terms of V_{BE}'s... We know that,

$$V_{BE1} = V_T \ln\left(\frac{I_{REF}}{I_S}\right) \quad \text{from} \quad I_C = I_S e^{\left(\frac{V_{BE}}{V_T}\right)}$$

$$V_{BE2} = V_T \ln\left(\frac{I_o}{I_S}\right)$$

• So, plug into the equation for I_o...

$$I_o R_E = V_T \ln\left(\frac{I_{REF}}{I_o}\right)$$

• To design a Widlar current source: 1) Choose I_{REF} and 2) Compute R_E knowing the I_o needed.

6: CURRENT MIRRORS

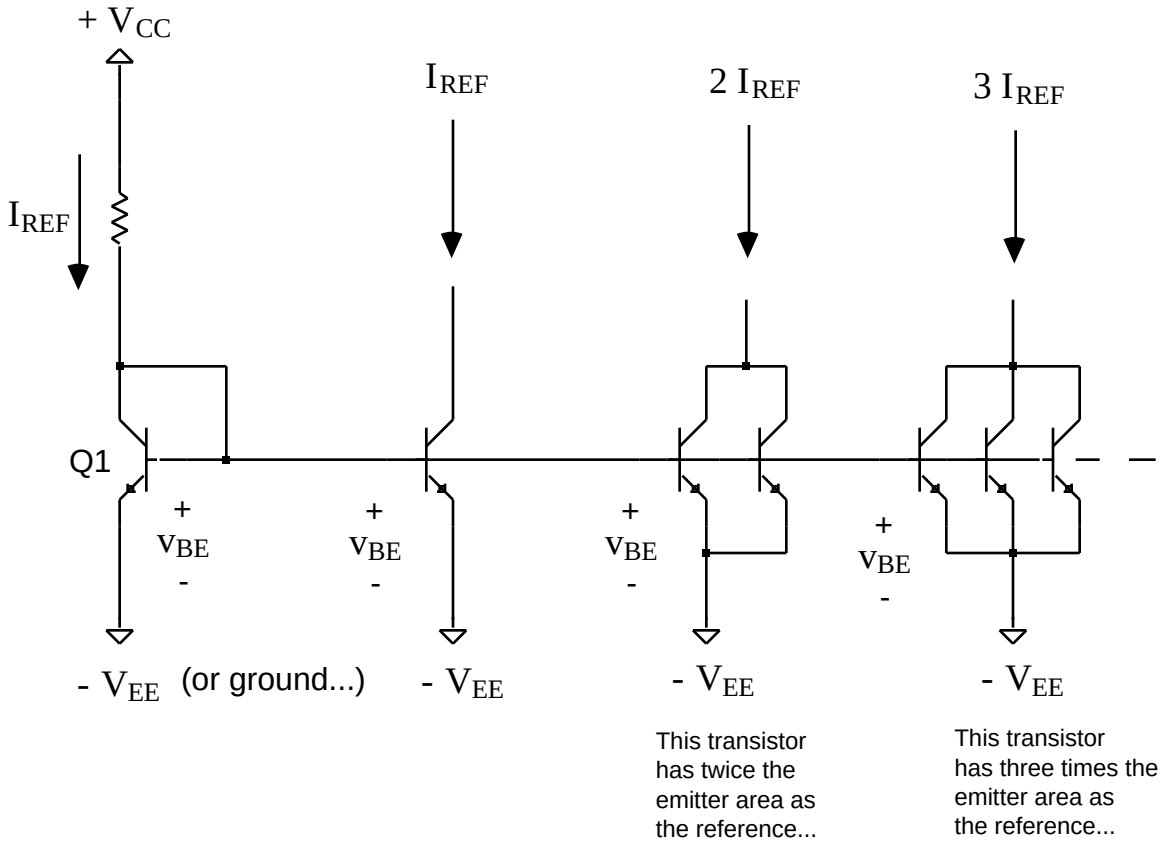
• This concept can easily be multiplied... You can use one diode-connected transistor to "steer" the current through many others by connecting their bases together...

• Since the collector current as a function of v_{BE} is given by,

$$I_C = I_S \, e^{\left(\frac{v_{BE}}{V_T}\right)}$$

• We can deliberately adjust I_S for any given transistor to control its I_C...

• I_S is a function of the area of the emitter, so in integrated circuits we can just make a bigger emitter to get more current....



7: NON-IDEALITIES OF BJT CURRENT SOURCES

• Real transistors are not ideal current sources!

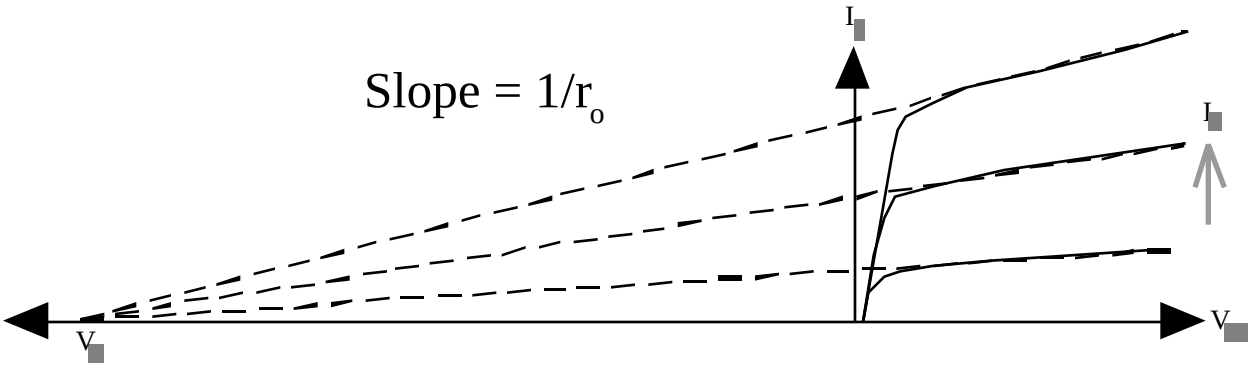
• Remember the Early Voltage and r_o?

• r_o is a resistance that models the slight effect of collector voltage on collector current in the active region of operation (the curves are not exactly flat!).

• r_o is inversely proportional to the DC bias current, so that as you increase I_C to get more g_m and more gain, you also get a lower (worse) resistance between the collector and emitter (i.e. the slope of the current/voltage curves is steeper).

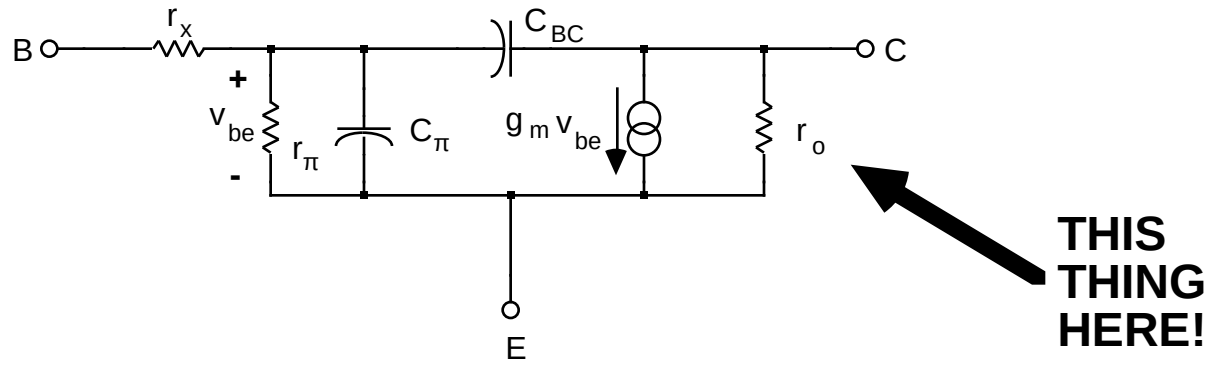
$$r_o = \frac{V_A}{I_C}$$

where V_A is the Early voltage... (see pages 207 - 208 in S & S)



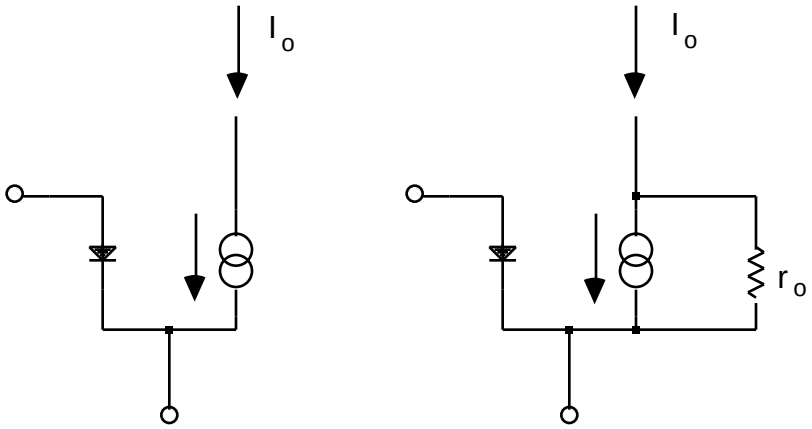
• Remember that in the above figure, the I_C versus V_{CE} curves represent equal base current steps between them.

• r_o is typically a **few thousand Ohms**...



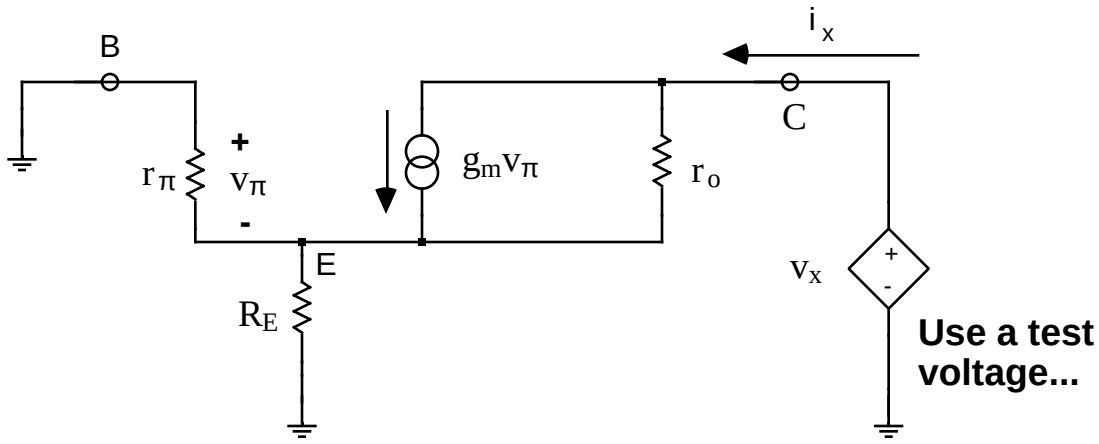
7.1 EFFECTS OF r_o ON CURRENT SOURCE PERFORMANCE

• An ideal current source has an infinite output resistance, but a “real” one with a BJT does not....



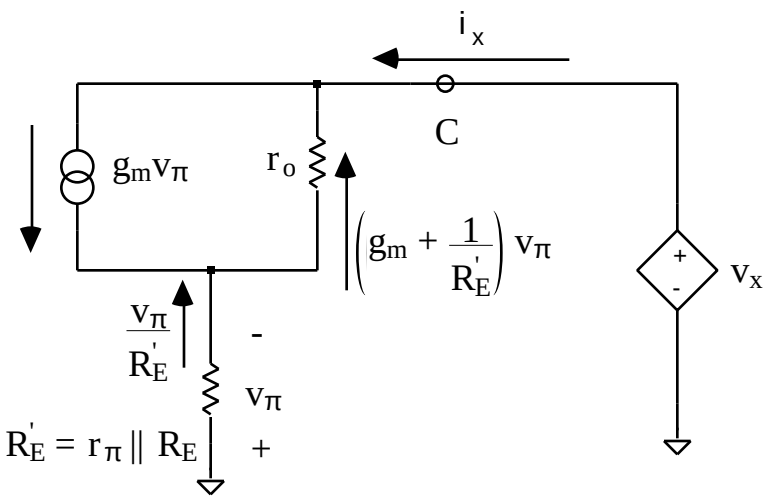
• We will see later that this means that you can’t simply “neglect” the bias current sources in your small-signal equivalent circuits if you want to get a detailed idea of performance....

• Try to find out what the output resistance of a BJT current source is (look at Widlar)...



• As usual, want to use Ohm’s Law to compute R_o...

• Use $R_E' = r_\pi \,||\, R_E$ and re-draw the circuit for clarity...



• The currents are relatively easy to see.... (careful with signs!)

$$i_x = g_m v_\pi - \left(g_m + \frac{1}{R_E'}\right) v_\pi = -\frac{1}{R_E'} v_\pi$$

• And the voltages can be summed around the loop to get v_x...

$$v_x = -v_\pi - \left(g_m + \frac{1}{R_E'}\right) v_\pi r_o$$

• Now you can go ahead and use Ohm's Law...

$$R_o \equiv \frac{v_x}{i_x} = \frac{1 + \left(g_m + \frac{1}{R_E'}\right) r_o}{\frac{1}{R_E'}} = R_E' + \left(1 + g_m R_E'\right) r_o$$

• Which, for small R_E' (where $R_E' = r_\pi \,||\, R_E$) gives (more intuitive)...

$$\boxed{R_o \approx \left(1 + g_m R_E'\right) r_o}$$

Chapter 13: MULTI-STAGE AMPLIFIERS

OW, OW, OW, OW!!!!
Berkeley EE student's thirty-third encounter with a soldering iron...

1: OBJECTIVE

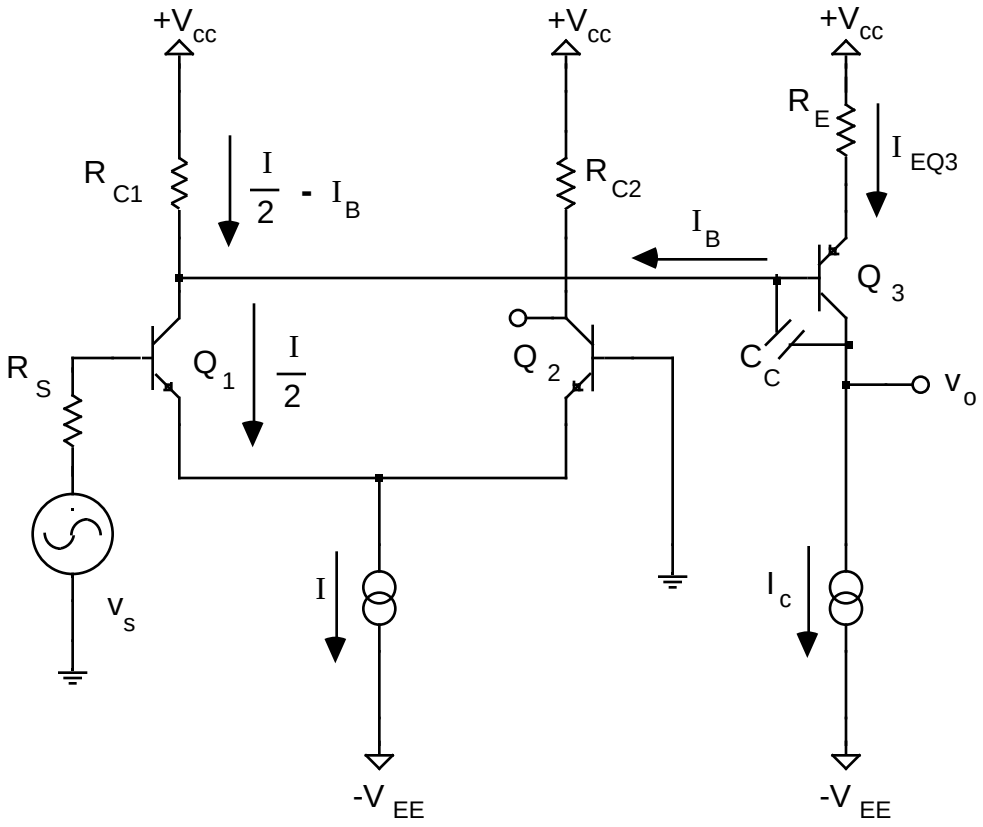
• To consider:

How to analyze and design multistage amplifiers based on the differential pair.

REVIEW SEDRA & SMITH SECTION 6.10

2: ANALYSIS OF AN EXAMPLE AMPLIFIER

• Begin with a simplified version of the EE122 discrete component op-amp....



• A small signal model for the differential pair with one input grounded has already been discussed, and is shown below.

• Looking at the output stage, there is emitter degeneration, and the load is also a function of R_o of the current source (R_o not shown above, but it is the output resistance of the current source driving Q_3) and the load resistance (R_L, not shown in the schematic)...

$$A_{voutput} \approx g_m' \left(R_L \parallel R_o \right)$$

• To evaluate the effect of the base current of Q_3 on the differential pair (tending to un-balance it), look at the voltages...

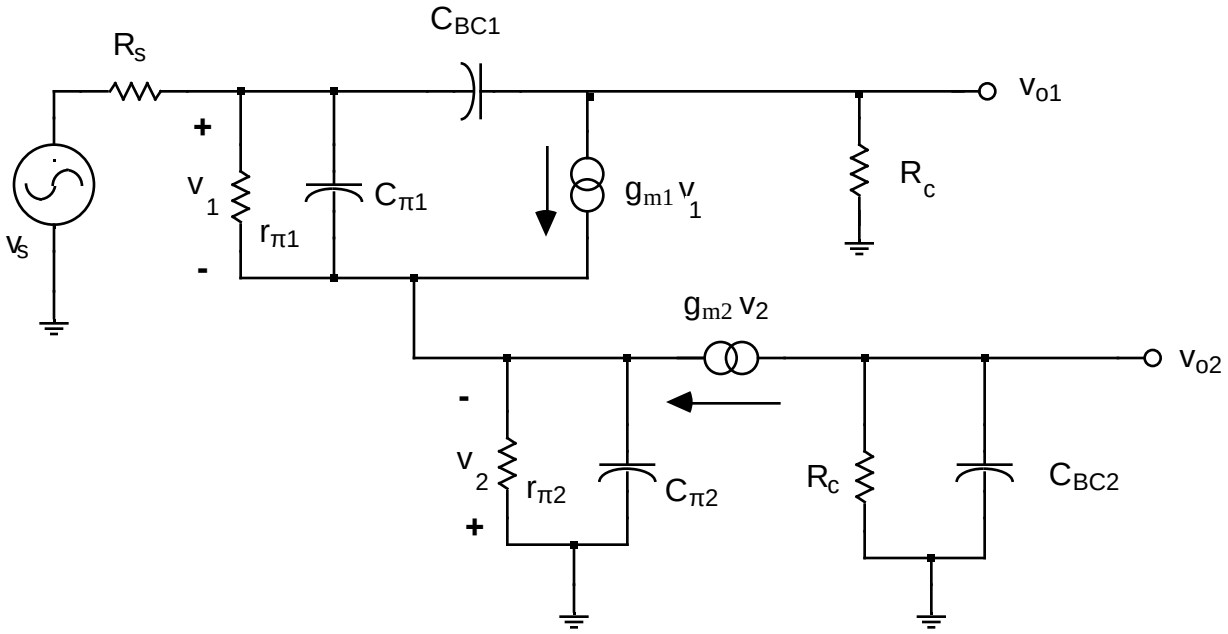
$$\left(\frac{I}{2} - I_B \right) R_{C1} = I_{EQ3} R_E - V_{BE3}$$

• One needs to compensate for the extra current flowing into Q_1! Do this by adjusting R_C's... THINK ABOUT THIS! To get balanced output voltages for the differential pair if one side has less current flowing in it (due to the base current of Q_3), that R_C can be made larger.

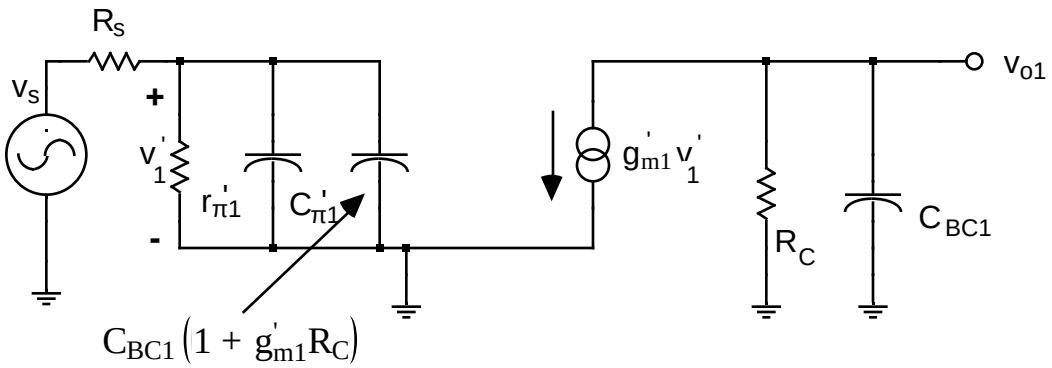
• Next consider the frequency response of this amplifier by considering it with one input grounded and using the model discussed in the Differential Amplifiers Chapter.

• For this situation, the common emitter amplifier formed by Q_1 has an emitter resistance of r_e (of Q_2) and drives the output stage formed by Q_3.

• We already looked at the response of the differential pair with one input grounded and arrived at a small-signal equivalent circuit like the one shown below:



• The signal path to v_{o1} was drawn as shown below, but now we will have to consider the loading effects of Q_3 on this circuit (not shown in the schematic immediately below),



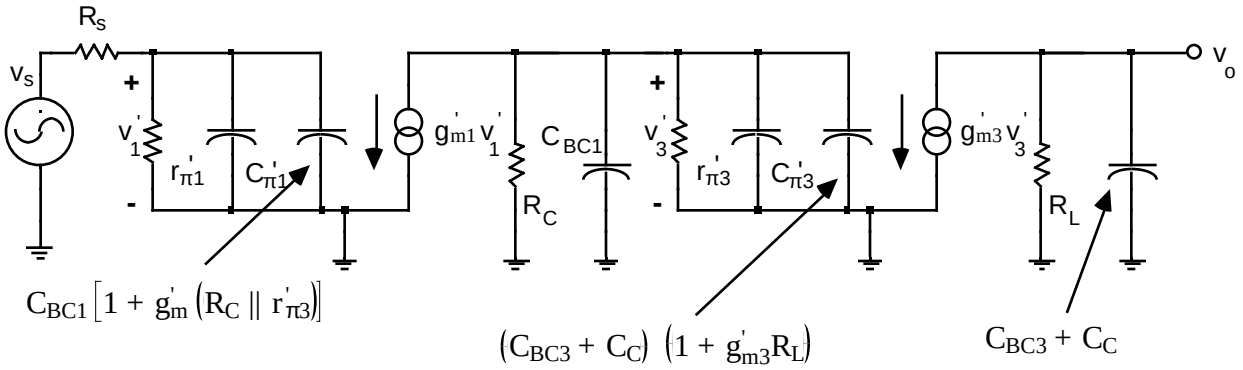
where $r_{\pi 1}' \approx 2r_{\pi 1}$ $C_{\pi 1}' \approx \frac{C_\pi}{2}$ $g_m' \approx \frac{g_{m1}}{2}$

• The output stage that is driven by v_{o1} must then be considered at this stage's load.

• This load includes the input resistance of the output stage in parallel with the R_C of Q_1 (otherwise the Miller approximation shown above will be incorrect since the gain at the transistor in question will change).

• The output is a common emitter amplifier with an un-bypassed emitter resistance R_E, and a collector resistance that is the output resistance of the current source (not shown in the simplified schematic at the beginning of this chapter).

• The input resistance of the output stage becomes the output load for the first stage.



Where,

$$r'_{\pi 1} = 2\, r_{\pi 1} \qquad g'_{m1} = \frac{g_{m1}}{2} \qquad r'_{\pi 3} = r_{\pi 3}\left(1 + g_{m3}\, R_E\right) \qquad g'_{m3} = \frac{g_{m3}}{\left(1 + g_{m3}\, R_E\right)}$$

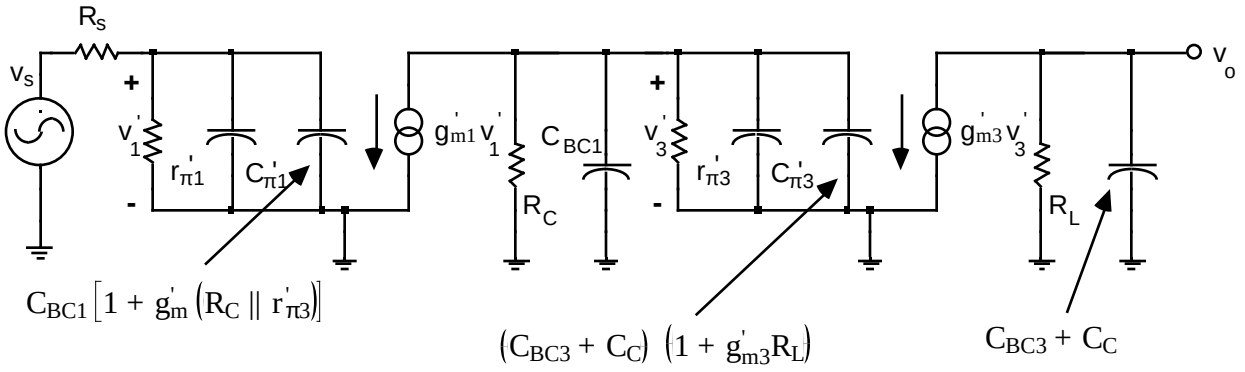
$$C'_{\pi 1} = \frac{C_{\pi 1}}{2} \qquad C'_{\pi 3} = \frac{C_{\pi 3}}{\left(1 + g_{m3}\, R_E\right)}$$

• For the mid-band gain (ignore the capacitances)...

$$A_M = \frac{r'_{\pi 1}}{R_S + r'_{\pi 1}} \left[g'_{m1}\left(R_C \parallel r'_{\pi 3}\right)\right]\left(g'_{m3}\, R_L\right)$$

Input voltage divider.... First-stage Gain... Second-stage Gain...

NOTE that this does *not* consider the current source output resistance (R_o) here, and if we did, it would be in parallel with R_L in the above equation. In the case above, the gain is a direct function of R_L.



• For the high frequency response, you need to consider the Miller multiplication of the capacitances in both stages...

• NOTE that the *compensation capacitor* C_C gets Miller multiplied too, as intended!!!

1) The input time constant is,

$$\left(R_S \parallel r_{\pi 1}'\right)\left(C_{\pi 1}' + C_{M1}\right) \quad \text{where} \quad C_{M1} = C_{BC1}\left[1 + g_{m1}'\left(R_C \parallel r_{\pi 3}'\right)\right]$$

Since R_S is typically very small, and thus corresponds to a very high frequency...

2) The inter-stage time constant is (for extra nerdiness we could include C_{BC1} but it is a relatively small contribution),

$$\left(r_{\pi 3}' \parallel R_C\right)\left(C_{\pi 3}' + C_{M3}\right) \quad \text{where} \quad C_{M3} = \left(C_{BC3} + C_C\right)\left(1 + g_{m3}' R_L\right)$$

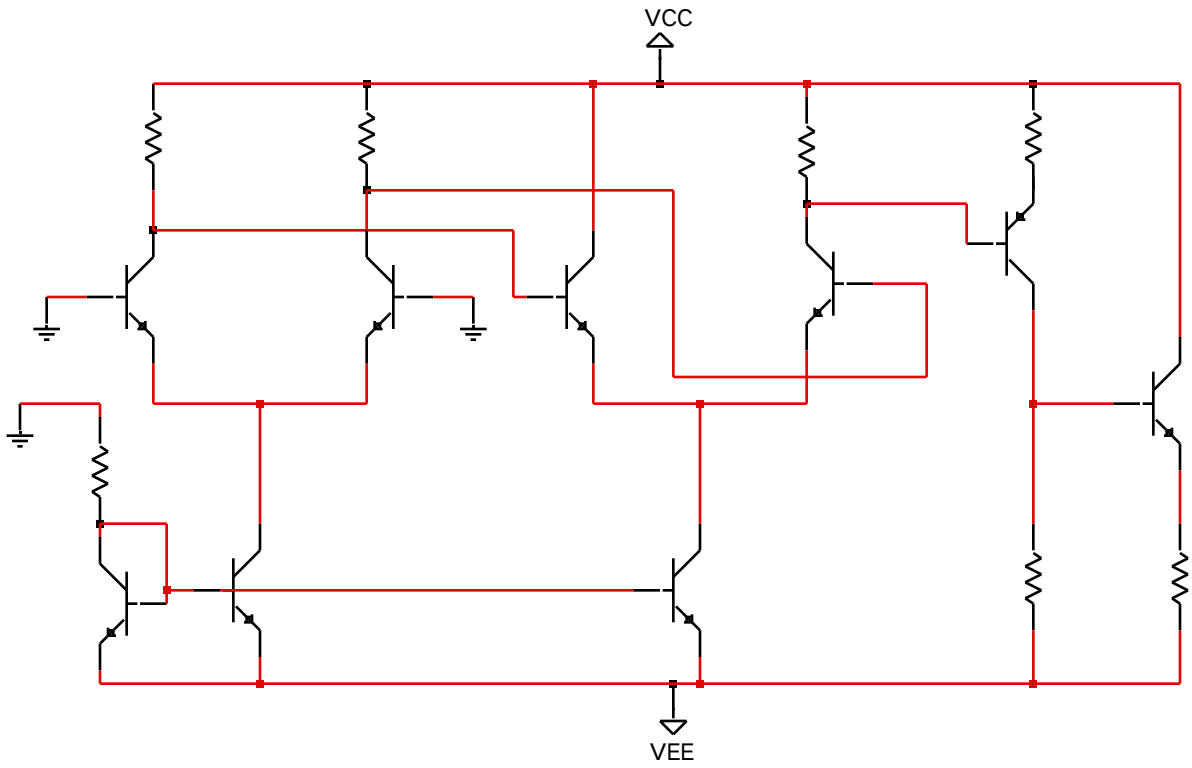
• This is a relatively long time constant because C_{M3} is very large (both C_{BC3} and C_C get Miller multiplied) and because the resistance here is moderate in magnitude.

3) And the output time constant is,

$$R_L\left(C_{BC3} + C_C\right)$$

• This time constant will be fairly short, but may be longer than the input circuit, depending on R_L , and external capacitances that may be in parallel with R_L.

• Look at the example in Sedra and Smith, page 438... First, look at it in chunks that are easy to understand (the reader may wish to add some lines and notations here)...



• Note the current mirrors to distribute current to the circuit, with the currents referenced to the resistor feeding the diode-connected transistor at lower left.

• Note the cascaded differential amplifier for increased gain (inputs are at the left, both shown grounded).

• Note that one of the transistors in the second differential amplifier has no collector resistor. It is not needed since no voltage is needed from this collector and it is the current there that is required for proper operation of the differential amplifier (the output beyond this point is single-ended, and the voltage from the second differential pair is taken at the other transistor, which does have a collector resistor).

• Note the PNP transistor used as an emitter degenerated common emitter stage just before the emitter follower output. If PNP transistors were not available, some other sort of level-shifter circuit (see below) would be necessary since the DC voltage in the signal path would otherwise be too close to V_{cc}.

3: LEVEL SHIFTERS

• In multi-stage amplifiers on integrated circuits, coupling capacitors between stages are almost always not used because they cannot be made large enough for reasonable low-frequency operation.

• Thus, stages are DC-coupled. This means that voltage offsets like V_{BE} drops between stages can start to add up... stages referred to as level shifters can be used to compensate where necessary.

• A typical level shifter is simply a degenerated CE amplifier (it can provide gain or simply act as an inverting buffer if $R_E = R_C$). The choice of R_C "programs" the quiescent collector voltage of the level shifter and can thus be used to "center" the output voltage of an op-amp so that it can swing both positive and negative from its quiescent point.

• Also, emitter followers and diodes can be used to drop ≈ 0.7 V per stage.

• By using PNP and NPN transistors, the *sign* of the voltage drop per shifter can be changed.

Chapter 14: FEEDBACK

.... by building an amplifier whose gain is made deliberately, say 40 decibels higher than necessary (10,000-fold excess on an energy basis) and then feeding the output back to the input in such a way as to throw away the excess gain, it has been found possible to effect extraordinary improvement in constancy of amplification and freedom from nonlinearity.

Harold Black, inventor of negative feedback, 1934

1: OBJECTIVES

• To consider:

The basics of feedback.

The properties of negative feedback.

The basic feedback topologies.

An example of the “ideal” feedback case.

Some realistic circuit examples and how to analyze them.

READ S&S Sections 8.1 - 8.7

2: INTRODUCTION TO FEEDBACK

• There are two types of feedback: ***regenerative*** (positive feedback) and ***degenerative*** (negative feedback).

• Unless you want your circuit to oscillate, we usually use ***NEGATIVE FEEDBACK***...

• This idea came about in the late 1920's when they were able to build amplifiers with reasonable gains, but with gains that were difficult to control from amplifier to amplifier...

• One day, while riding the Staten Island Ferry, Harold Black invented negative feedback....

2.1 PROPERTIES OF NEGATIVE FEEDBACK

• The gain of the circuit is made less sensitive to the values of individual components.

• Nonlinear distortion can be reduced.

• The effects of noise can be reduced (but not the noise itself).

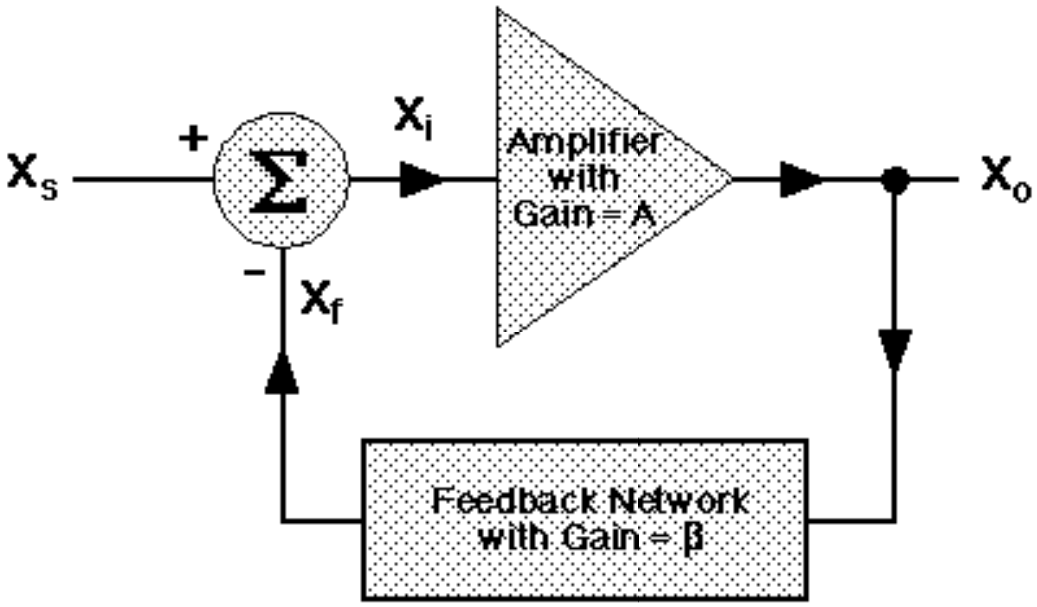
• The input and output impedances of the amplifier can be modified.

• The bandwidth of an amplifier can be extended.

• All you have to do to "get some feedback" (of the negative kind) is to supply a scaled replica of the amplifier's output to the inverting (negative) input (more on this below) and *presto*!

• Of course, if you use negative feedback, overall gain of the amplifier is always less than the maximum achievable by the amplifier without feedback.

2.2 THE BASIC FEEDBACK CIRCUIT



• With an input signal x_s, an output signal x_o, a feedback signal x_f, and an amplifier input signal x_i, let's look at the basic feedback circuit illustrated above.

• The amplifier has a gain of A and the feedback network has a gain of β...

• The input to the amplifier is,

$$x_i = x_s - x_f$$

• The output of the amplifier is,

$$x_o = Ax_i$$

• So we can obtain an expression for the output signal in terms of the input signal and the feedback gain...

$$x_o = A\left(x_s - x_f\right) = A\left(x_s - \beta x_o\right)$$

• Rearranging,

$$x_o = Ax_s - A\beta x_o \qquad \rightarrow \qquad x_o\left(1 + A\beta\right) = Ax_s$$

• From which we obtain the negative feedback equation by solving for the overall gain $\frac{x_o}{x_s}$,

$$A_{fb} \equiv \frac{x_o}{x_s} = \frac{A}{1 + A\beta}$$

• ***This means that the gain is almost entirely determined by the feedback circuit!!!***

$$A_{fb} \equiv \frac{x_o}{x_s} = \frac{A}{1 + A\beta} \approx \frac{1}{\beta} \qquad \text{for large A}$$

• For positive feedback, you only need to change the "+" sign in the denominator to a "-" sign....

• It is easy to obtain the equation for the feedback signal, x_f,

$$x_f = \frac{A\beta}{1 + A\beta} x_s$$

• If the amplifier gain and the loop gain are **large** (i.e. $A\beta >> 1$), then the feedback signal x_f becomes **nearly an identical copy** of the input signal x_s....

• ***This explains why the two terminals of an op-amp become nearly identical when using negative feedback...*** (Remember the "virtual ground" stuff?)

3: HOW FEEDBACK AFFECTS BANDWIDTH

• Assuming an amplifier with a single-pole frequency response (i.e. an “ideal” op-amp), its frequency response is given by,

$$A(s) = \frac{A_M}{1 + \frac{s}{\omega_H}}$$

• If you use the amplifier with negative feedback, the gain becomes,

$$A_f(s) = \frac{A(s)}{1 + \beta A(s)}$$

• Substituting, you get,

$$A_f(s) = \frac{\frac{A_M}{(1 + A_M\beta)}}{1 + \frac{s}{\omega_H(1 + A_M\beta)}}$$

• Thus we have another single-pole response, but with a high cut-off frequency given by,

$$\omega_{Hf} = \omega_H(1 + A_M\beta)$$

• THIS MEANS THAT THE UPPER CUT-OFF FREQUENCY IS INCREASED BY A FACTOR EQUAL TO THE AMOUNT OF FEEDBACK.

THIS IS THE FUNDAMENTAL GAIN-BANDWIDTH PRODUCT TRADE-OFF THAT WE STUDIED WITH OP-AMPS!!!

• The same is true for the lower cut-off frequency, and the amplifier will have a lower cut-off frequency by a factor again equal to the amount of feedback,

$$\omega_{Lf} = \frac{\omega_L}{1 + A_M\beta}$$

THE BANDWIDTH IS EXTENDED BY THE SAME AMOUNT THE MID-BAND GAIN IS DECREASED.

• A KEY ASSUMPTION HERE IS THAT THE SOURCE, LOAD AND FEEDBACK NETWORK DO NOT AFFECT THE GAIN OF THE AMPLIFIER!

• IN PRACTICE THIS WILL NOT BE THE CASE, SO WE WILL LEARN HOW TO TAKE AMPLIFIER LOADING INTO CONSIDERATION.

FUNDAMENTAL ASSUMPTIONS:

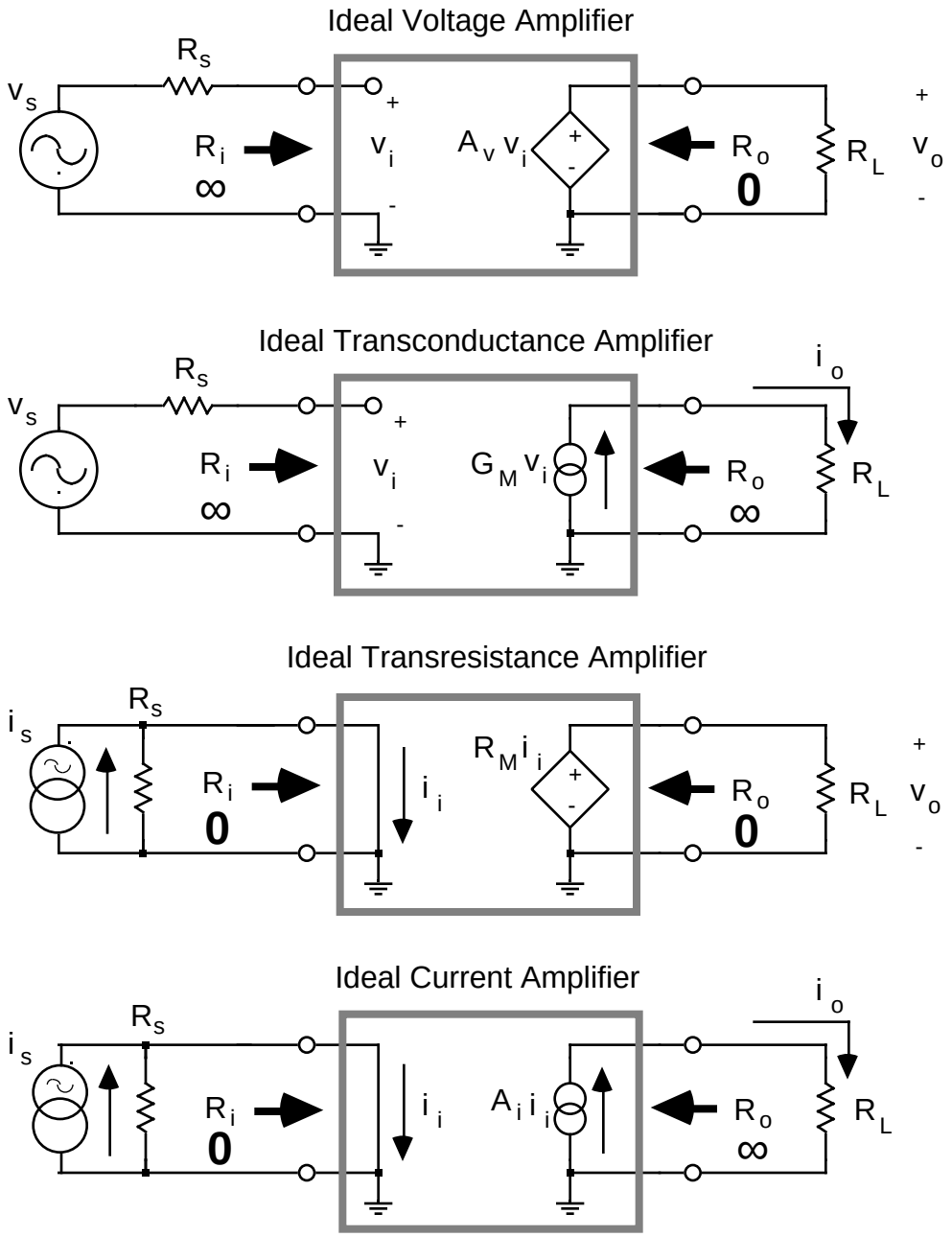
1) The feedback network is **UNILATERAL**. This means that it transmits signals only one way (from output to input of the composite circuit). This is usually only approximately true.

2) The amplifier is **UNILATERAL**. This means that it transmits signals only one way (from the input to the output of the composite circuit).

3) The loop gain, β, is **INDEPENDENT** of the load and source resistances seen by the composite circuit.

4: FROM BASIC BLOCK DIAGRAM TO ACTUAL FEEDBACK CIRCUITS

4.1 REMINDER: TYPES OF AMPLIFIERS



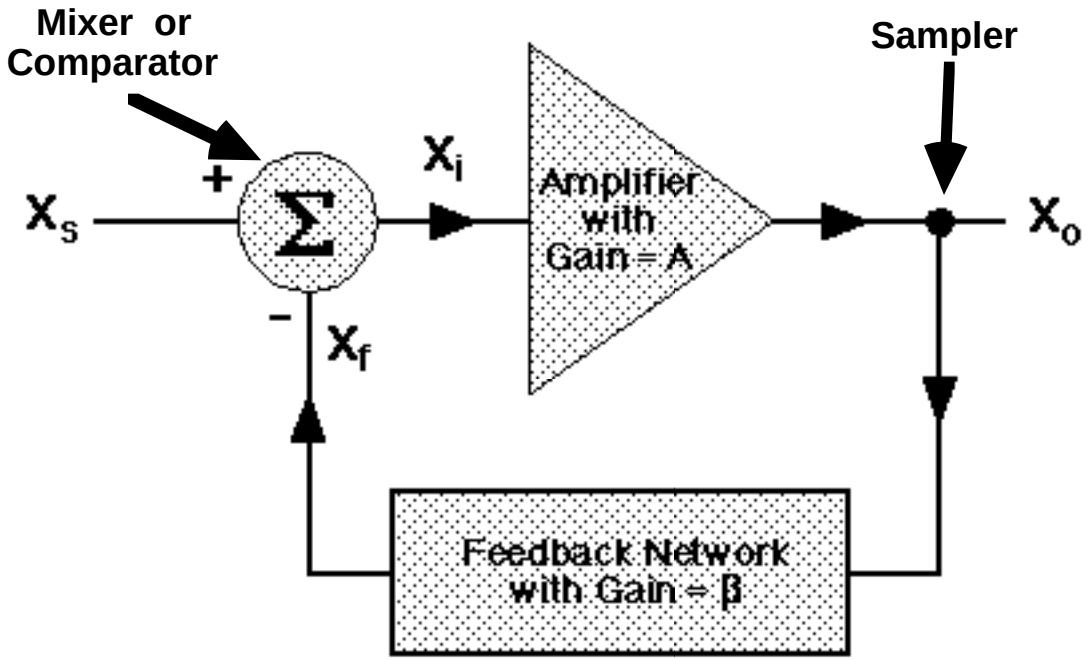
NOTE THAT THE *IDEAL* INPUT AND OUTPUT RESISTANCES ARE SHOWN.

Type of Amplifier	Gain Expression	Ideal Input Impedance	Ideal Output Impedance
Voltage	$A_v = \frac{v_o}{v_s}$ = voltage gain (dimensionless)	$Z_i = \infty$	$Z_o = 0$
Transconductance	$G_m = \frac{i_o}{v_s}$ = transconductance in Ω^{-1} or Siemens	$Z_i = \infty$	$Z_o = \infty$
Transresistance	$R_m = \frac{v_o}{i_s}$ = transresistance in Ω	$Z_i = 0$	$Z_o = 0$
Current	$A_i = \frac{i_o}{i_s}$ = current gain (dimensionless)	$Z_i = 0$	$Z_o = \infty$

• The distinction between types of amplifiers is essential because the type of feedback used with each type is distinct and requires analysis in the “native” units of current or voltage that is used for input and output.

THIS STUFF IS EASY TO GET CONFUSED ON!!! PLEASE SPEND A LITTLE TIME TO TRY TO MEMORIZE THE DIFFERENT AMPLIFIER TYPES AND THE RELEVANT FEEDBACK TOPOLOGIES...

4.2 BASIC STRUCTURE OF THE CIRCUIT



• Here we have assumed that there was an input "comparator" or "mixer" and an output "sampler" that provided us with a copy of the output signal for use as a feedback signal.

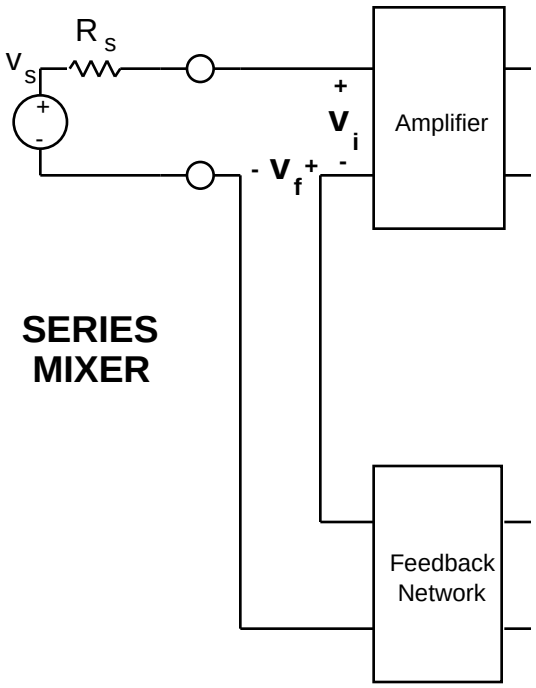
• The form these devices take depends upon whether the amplifier's input and output are current or voltage based...

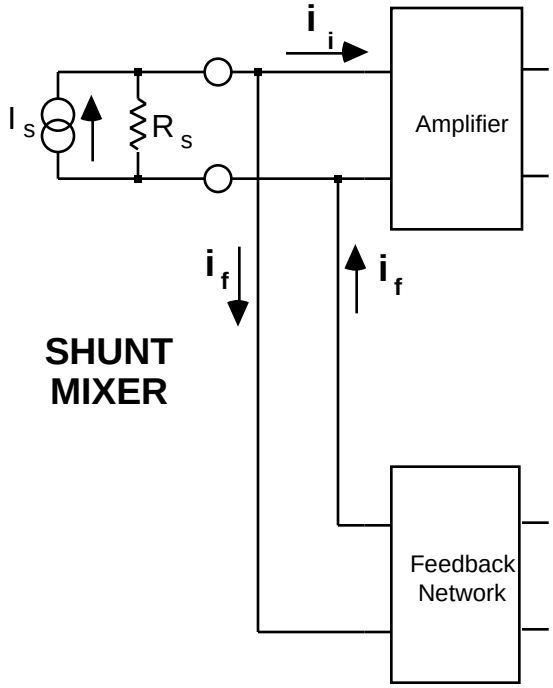
FOOD FOR THOUGHT...

• If x_o decreases due to negative feedback, won't βx_o also decrease, making the output eventually go to zero????

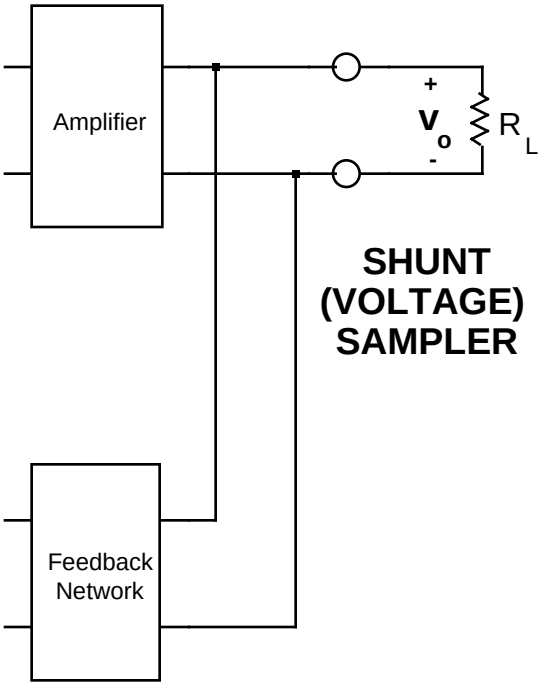
• **NO!** This is because subtracting $x_f = \beta x_o$ causes x_i to decrease slightly so βx_o decreases slightly so x_i is allowed to **INCREASE** slightly! This acts to stabilize the gain!

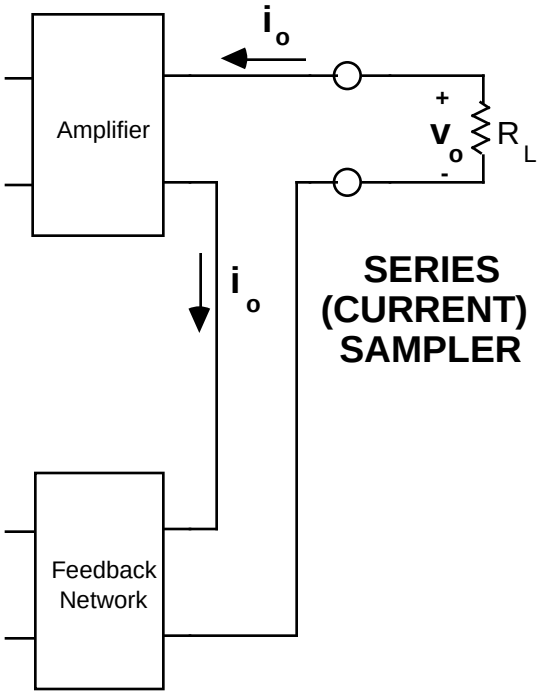
4.3 TYPES OF MIXER





4.4 TYPES OF SAMPLER





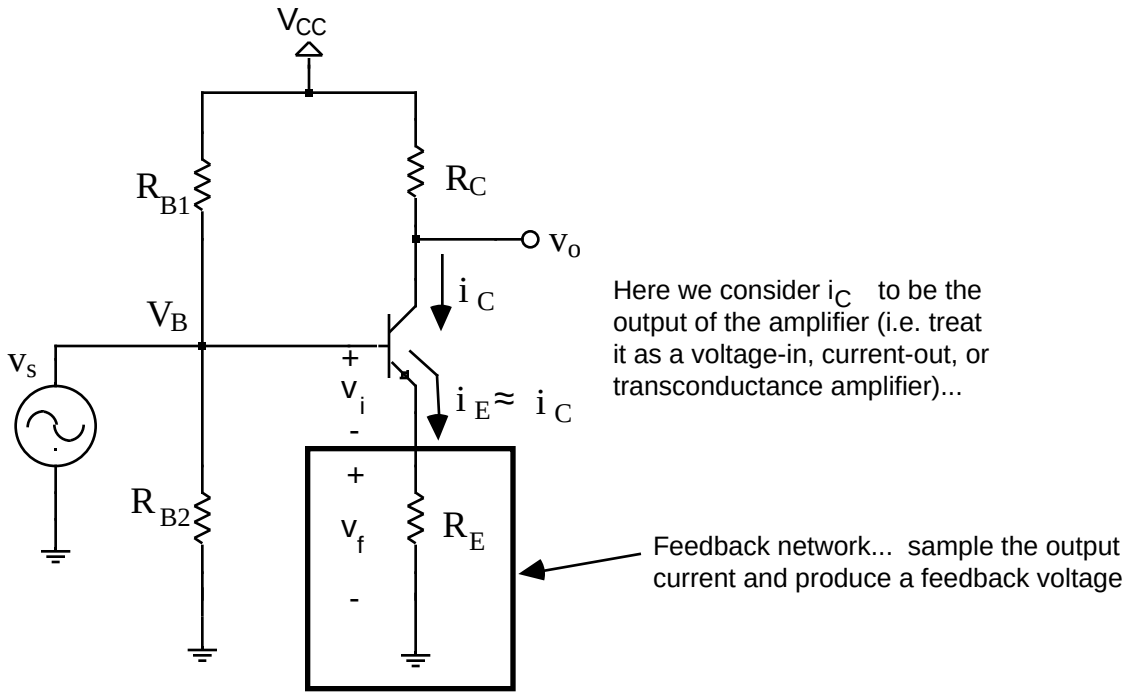
NOTE the effect of feedback on input and output impedance is just a function of the mixing and sampling type, respectively... e.g. if you put something in series with the input, its impedance goes up... it goes down if you put something in shunt (same idea at the output).

• We refer to a given feedback amplifier in terms of the “MIXING - SAMPLING” feedback, where MIXING and SAMPLING are either SHUNT or SERIES...

• There are four possible types... (for sampling think of how you would measure I or V in the lab... series for current and shunt for voltage).

INPUT-OUTPUT (MIXING - SAMPLING)		
SERIES-SHUNT	series (voltage) mixing, voltage-sampling	V-V
SHUNT-SERIES	shunt (current) mixing, current-sampling,	I-I
SERIES-SERIES	series (voltage) mixing, current-sampling	V-I
SHUNT-SHUNT	shunt (current) mixing, voltage-sampling	I-V

• Let's consider a familiar example.... the **degenerated common-emitter amplifier**.



• Since we **sample** the output **current** and **generate** a **voltage feedback** signal, this is a **series-series** feedback topology.

• Considering the output current to be the output signal (e.g. $i_o = i_c$) and the input to be v_s (for simplicity, assume that R_{B1} and R_{B2} are very large), the units of the basic amplifier are,

$$\text{Overall Gain} = A = \frac{i_o}{v_s} \equiv G_m \text{ in } \Omega^{-1}$$

• We know that the feedback voltage is given by Ohm's Law as,

$$v_f = i_o R_E \quad \left(\text{ so the feedback network gain, } \beta = R_E \right)$$

(**NOTE**: **don't get confused!** This ß is **NOT** the transistor's ß!)

$$\text{Transistor's current gain} = \frac{i_o}{v_i} \equiv g_m \text{ in } \Omega^{-1}$$

• The output current is given by,

$$i_o = g_m (v_s - v_f) = g_m (v_s - i_o R_E)$$

• Combining these equations to find the overall gain for the amplifier, G_m, we end up with an equation we have seen before!

$$G_m = \frac{i_o}{v_s} = \frac{g_m (v_s - i_o R_E)}{v_s} = g_m \left(1 - \frac{i_o}{v_s} R_E\right) = g_m (1 - G_m R_E) = g_m - g_m G_m R_E$$

$$G_m (1 + g_m R_E) = g_m$$

$$G_m = \frac{g_m}{(1 + g_m R_E)} \qquad \text{THIS IS } g'_m \text{ THAT WE SAW BEFORE!}$$

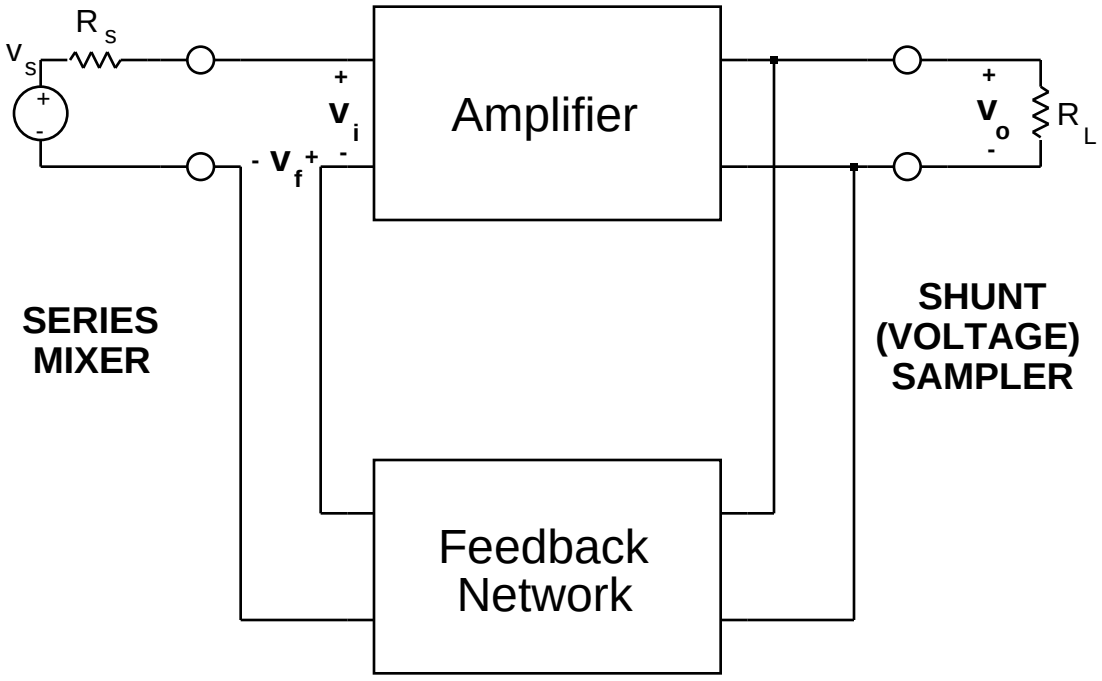
Note that,

$$G_m = \frac{g_m}{(1 + g_m R_E)} = \frac{A}{1 + A\beta}$$

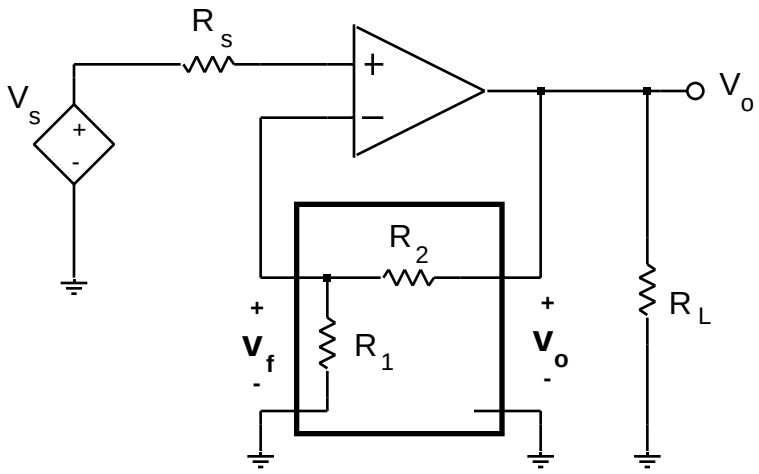
(Again, this ß is not ß for the transistor!)

5: SERIES-SHUNT FEEDBACK -> VOLTAGE AMP

(SERIES [VOLTAGE] MIXING, VOLTAGE-SAMPLING)



• An “ideal” example... The non-inverting op-amp configuration using an ideal op-amp (infinite input impedance, zero output impedance)...



• Notice how you can re-draw the two feedback resistors as a feedback network of the form we are discussing...

• Note that there are often “implied” ground connections to make the feedback network a four-terminal device...

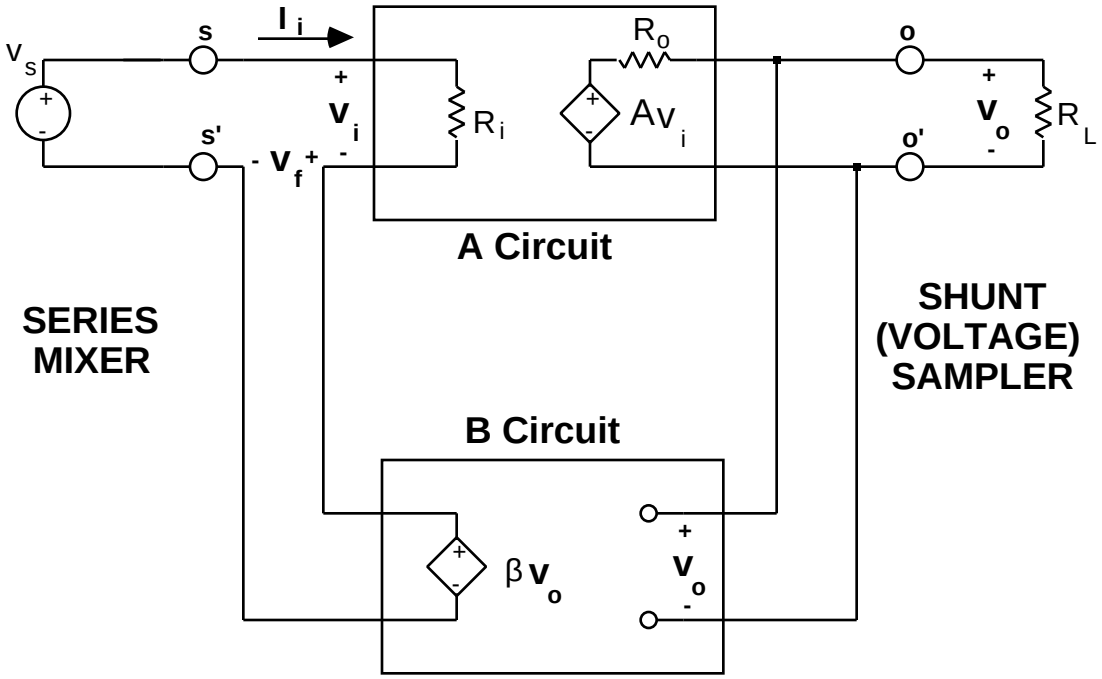
• The feedback network gain can be obtained directly by voltage division,

$$\beta = \frac{R_1}{R_1 + R_2}$$

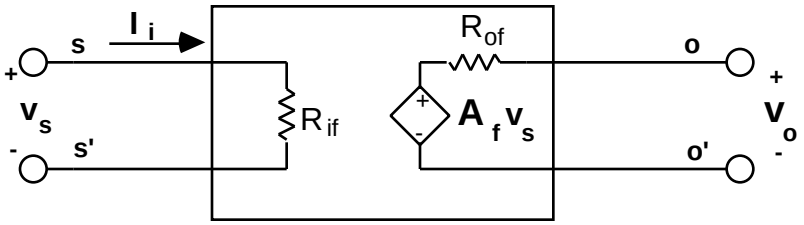
• This can be plugged into the feedback gain equation to find the overall gain,

$$A_{fb} \equiv \frac{x_o}{x_s} = \frac{A}{1 + A\left(\frac{R_1}{R_1 + R_2}\right)} \approx \frac{1}{\left(\frac{R_1}{R_1 + R_2}\right)} = \left(1 + \frac{R_2}{R_1}\right)$$

• Continuing with the series-shunt case, but including the input and output resistance terms (R_i and R_o),



Equivalent Circuit



• We can obtain an expression for the equivalent input and output resistance...

$$R_{if} \equiv \frac{V_s}{I_i} = \frac{V_s}{\left(\frac{V_i}{R_i}\right)} = R_i \frac{V_s}{V_i} = R_i \frac{V_i + \beta A V_i}{V_i} = R_i \left(1 + A\beta\right)$$

(V_f = $\beta A V_i$)

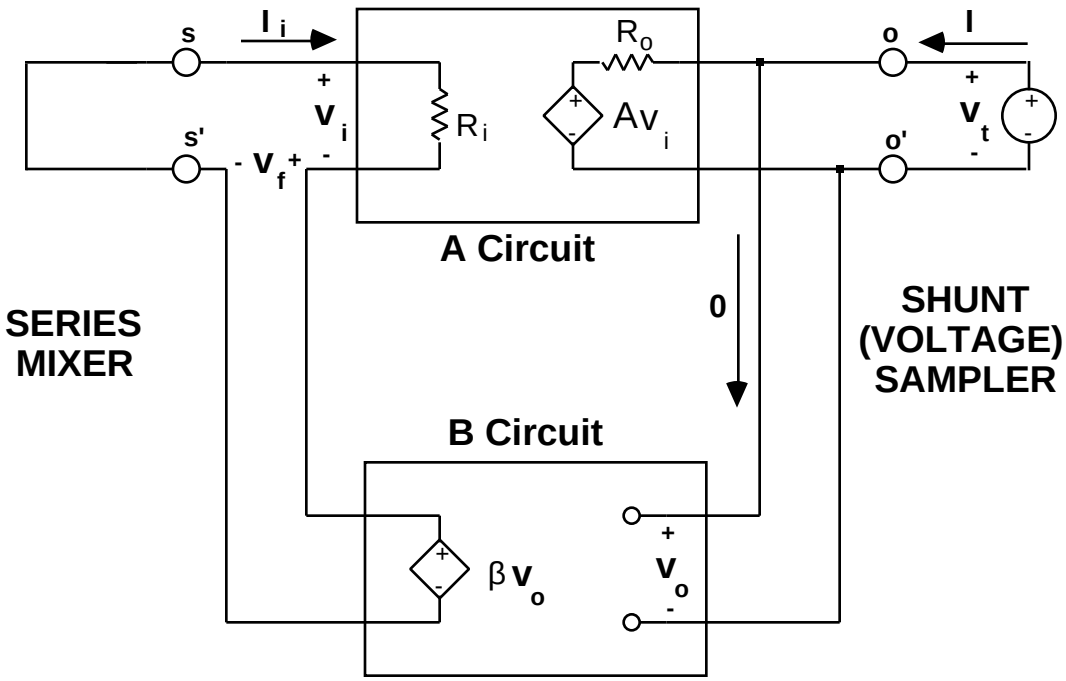
• **NOTE** that later on, we will generalize this to include **IMPEDANCES**....

$$Z_{if}(S) = Z_i(S)\left[1 + A(S)\,\beta(S)\right] \quad \text{(always true for series mixing)}$$

• The effect of feedback on input resistance or impedance is only a function of the method of mixing

• The output resistance can also be obtained by the same method we used previously:

• Reduce the input signal (V_s) to zero and apply a test voltage V_t at the output....



• **Note** that you "kill" the input voltage by shorting the input terminals.

• Starting with the definition,

$$R_{of} \equiv \frac{V_t}{I} \quad \rightarrow \quad I = \frac{V_t - AV_i}{R_o}$$

• Since $V_s = 0$,

$$V_i = -V_f = -\beta V_o = -\beta V_t$$

• Thus,

$$I = \frac{V_t - AV_i}{R_o} = \frac{V_t + A\beta V_t}{R_o}$$

• Therefore,

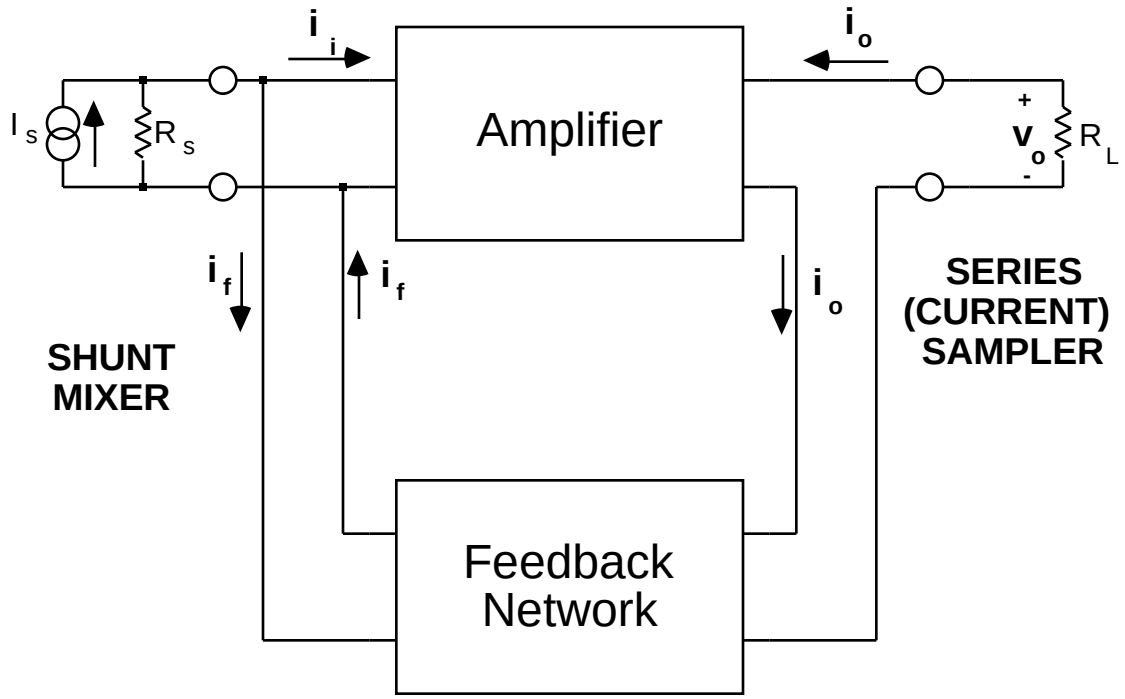
$$R_{of} = \frac{R_o}{1 + A\beta} \quad \text{or, more generally,} \quad Z_{of} = \frac{Z_o}{1 + A\beta}$$

True for all shunt sampling cases.

• Again, this could be written with frequency-dependent A and β...

6: SHUNT-SERIES FEEDBACK -> CURRENT AMP

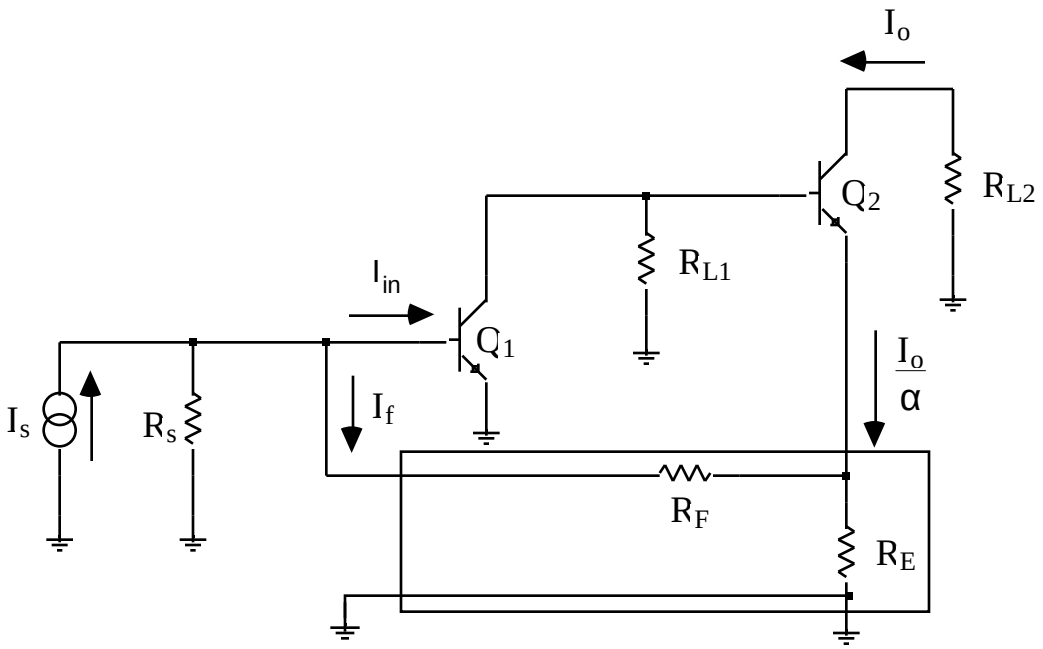
(SHUNT [CURRENT] MIXING, CURRENT-SAMPLING)



• Here we have series sampling (like connecting an ammeter in series with a circuit in which you want to know the current flow)...

• Shunt mixing feeds back a β-scaled version of the sampled current...

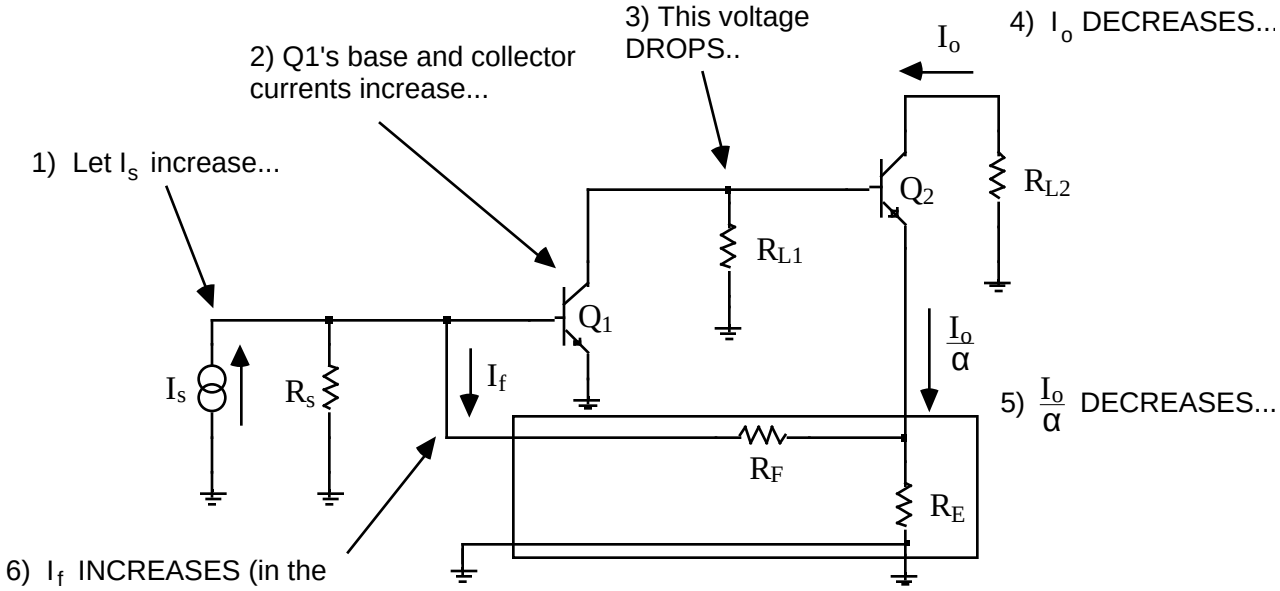
• Now look at a practical circuit example, a two-stage common-emitter amplifier.



• NOTE that the feedback current, I_f is shown SUBTRACTING from the input current... This is the notation we will use!

• BE SURE TO "GO AROUND THE LOOP" to verify that the polarity of the feedback is negative (this means that the loop gain (1 + Aβ) must be positive...)

'ROUND THE LOOP....



CONCLUSION: the feedback is negative since the increase in I_f SUBTRACTS from I_s .....

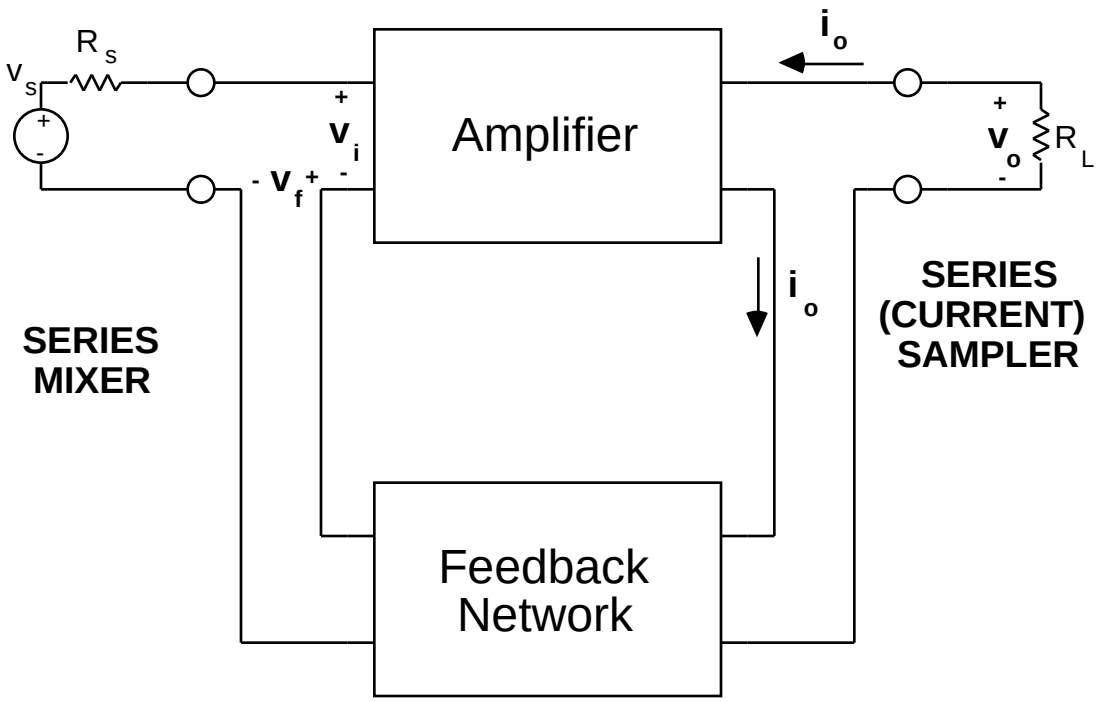
• This sort of “sanity check” tends to be essential....

• Note that here we did not sample the OUTPUT current directly, but rather the nearly equal emitter current of Q_2... This is quite reasonable, and we will do this in the next example too....

7: SERIES-SERIES FEEDBACK -> TRANSCONDUCTANCE AMPLIFIER

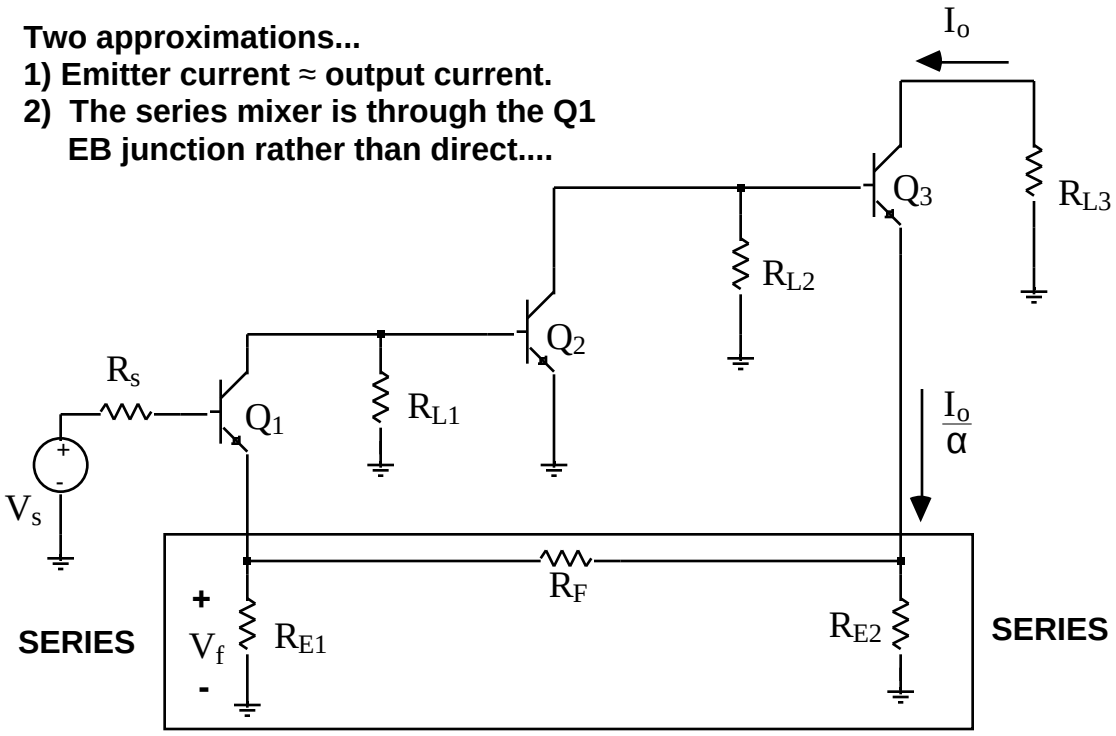
VOLTAGE-IN, CURRENT-OUT

(SERIES [VOLTAGE] MIXING, CURRENT-SAMPLING)



• This type of circuit is used when you need to generate an output current proportional to a command voltage, such as when you need to drive the deflection coils in a television...

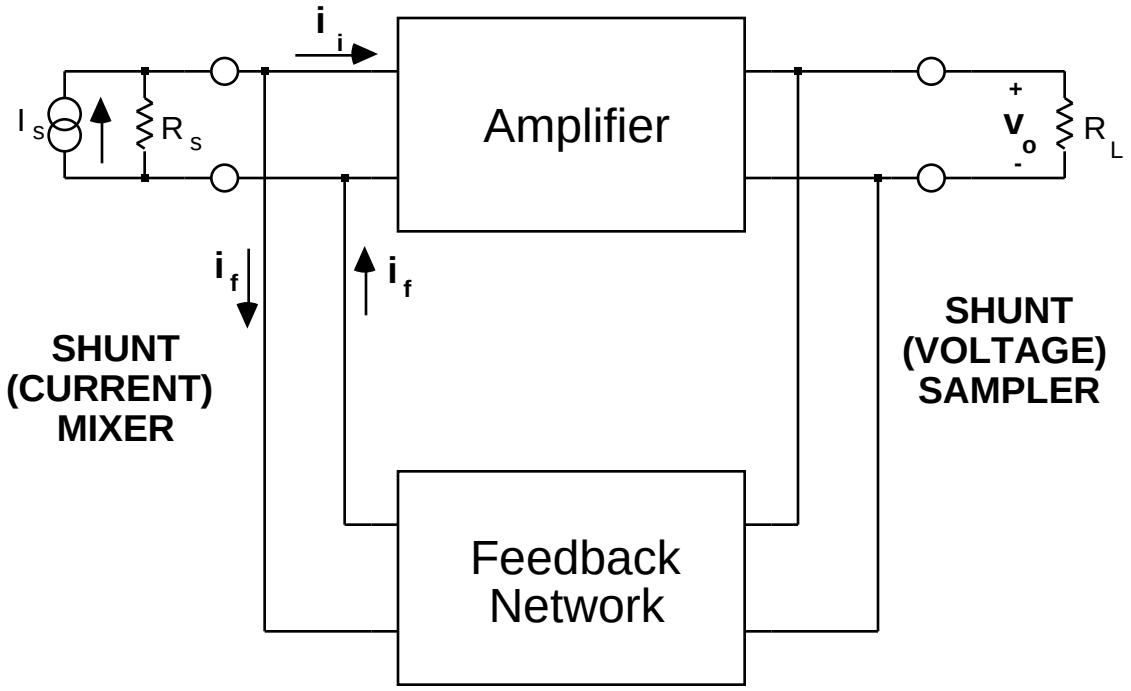
Two approximations...
1) Emitter current ≈ output current.
2) The series mixer is through the Q1 EB junction rather than direct....



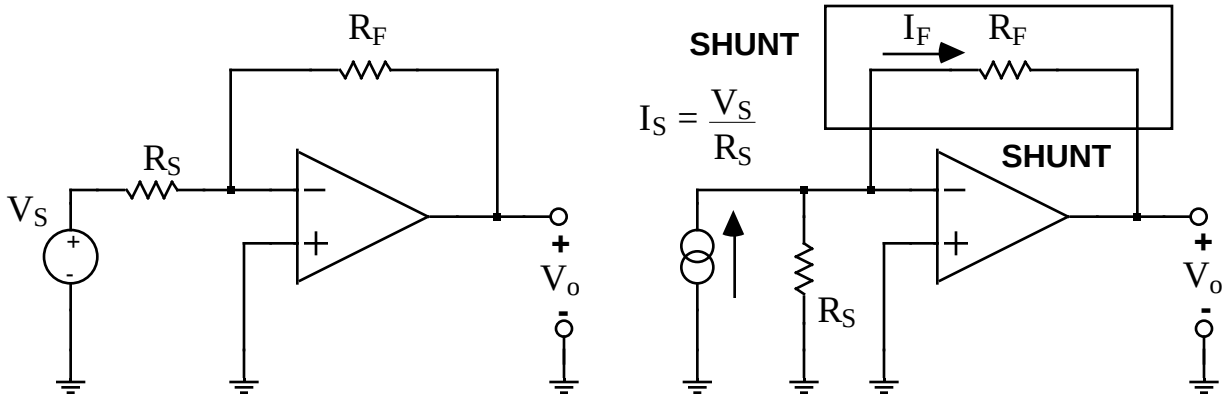
8: SHUNT-SHUNT FEEDBACK -> TRANSRESISTANCE AMPLIFIER

CURRENT-IN, VOLTAGE-OUT

(SHUNT [CURRENT] MIXING, VOLTAGE-SAMPLING)



• If you re-draw the inverting op-amp configuration with a Norton input source, you can treat the circuit as a transresistance amplifier....



• 'Round the loop... If I_S increases, V_o decreases, allowing I_F to increase. I_F subtracts from I_S, so an increased I_F means negative feedback (as you expected, I hope!)....

9: FEEDBACK ANALYSIS IN REALISTIC CIRCUITS

• In real situations, the feedback network is generally passive, and loads the basic amplifier in the loop and thus affects A, R_i and R_o....

• The source and load resistances will also affect these three parameters...

• The trick is to lump these “bad” effects ***into*** the previously mentioned “A” circuits (and sometimes “β” circuits, but we lump it all into "A" here)....

• These “lumped” circuits can be plugged into the ideal feedback circuit case and used to determine the properties of the closed-loop case....

• For each of the four feedback topologies, there is a set of rules about how to incorporate the loading effects and how to compute β.

9.1 SUMMARY OF STEPS YOU WILL USE

1) Re-draw the amplifier as an "A" circuit which takes into account the fact that introducing the feedback network actually affects the open-loop gain of the amplifier! Also lump R_S and R_L into the "A" circuit. The fact that this loading occurs means that you can't just use,

$$A_f = \frac{A}{1 + A\beta}$$

until you compute a new "A" value that takes into account the loading!!!

2) After determining the "A" circuit, find the value for β.

3) Now use the corrected "A" gain (call it A') to compute A_f ...

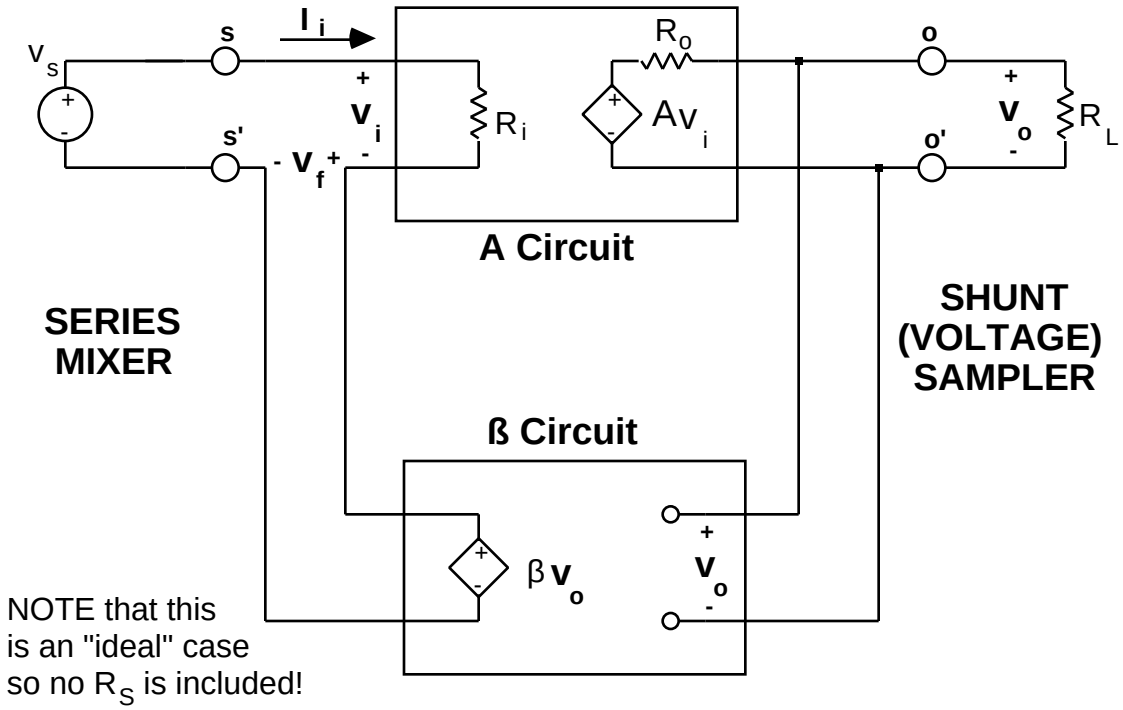
$$A_f = \frac{A'}{1 + A'\beta}$$

4) Now, if you need to, you can compute the input and output impedances (with feedback) using the appropriate (1 + A'β) scaling (how to do this is explained below).

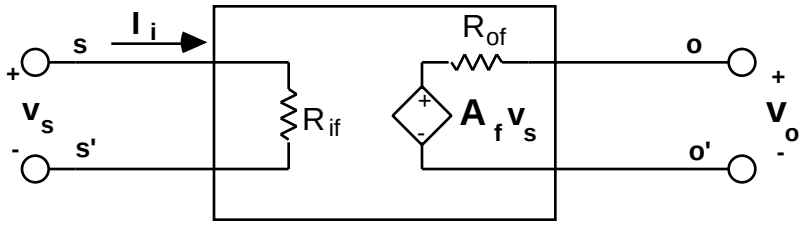
5) Also, if you need to, you can compute the input and output impedances of the amplifier (with feedback) looking into its terminals but without R_S and R_L (see below). You simply mathematically remove the effects of R_S and R_L. Why not just start without them? The reason is that you have to take into account their loading effects on the amplifier ***BEFORE*** doing the feedback calculations.

10: SERIES-SHUNT FEEDBACK

(SERIES [VOLTAGE] MIXING, VOLTAGE-SAMPLING)



Equivalent Circuit



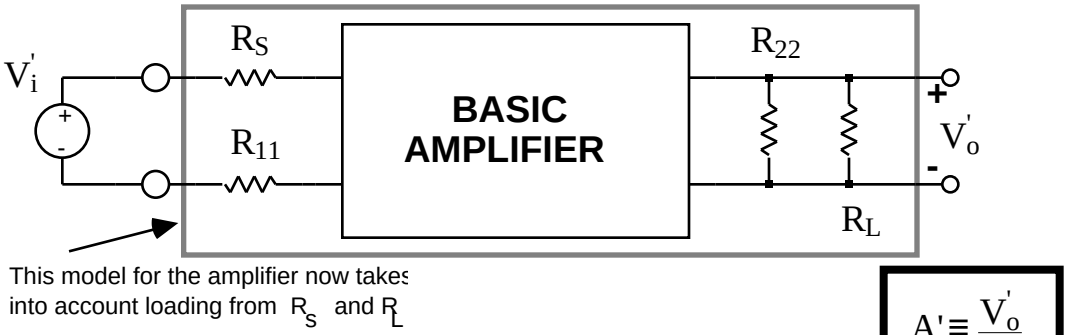
• The above equivalent circuit is the "goal," incorporating all of the effects of loading and feedback into a final equivalent.

• We will learn a general set of rules (one for each of the four types of feedback configurations) to "pull" the effects of R_S, R_L and ß-network loading into the a new "A" circuit and then apply the basic feedback equation with the ß-network taken to be "ideal."

• Determine the loading effects on input and output by “destroying” the feedback from each end of the feedback network to the other...

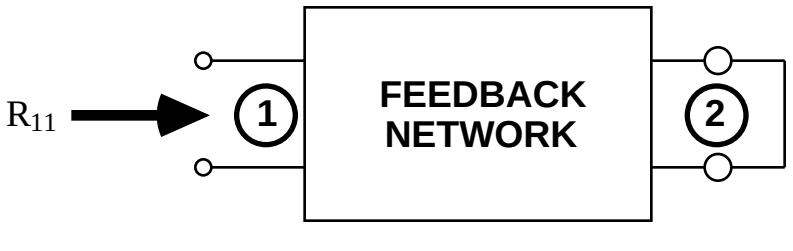
SHORT SHUNTS and SEVER SERIES

RULES FOR SERIES-SHUNT



This model for the amplifier now takes into account loading from R_S and R_L

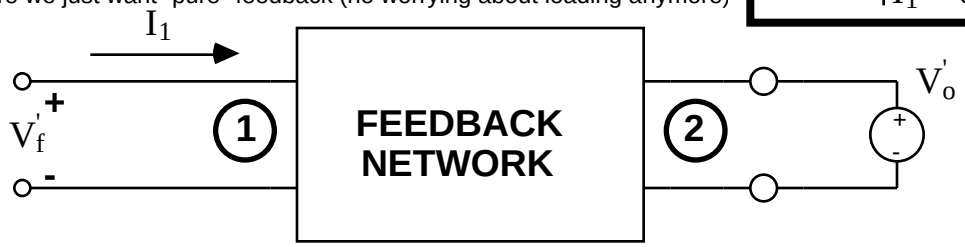
$$A' \equiv \frac{V_o'}{V_i'}$$



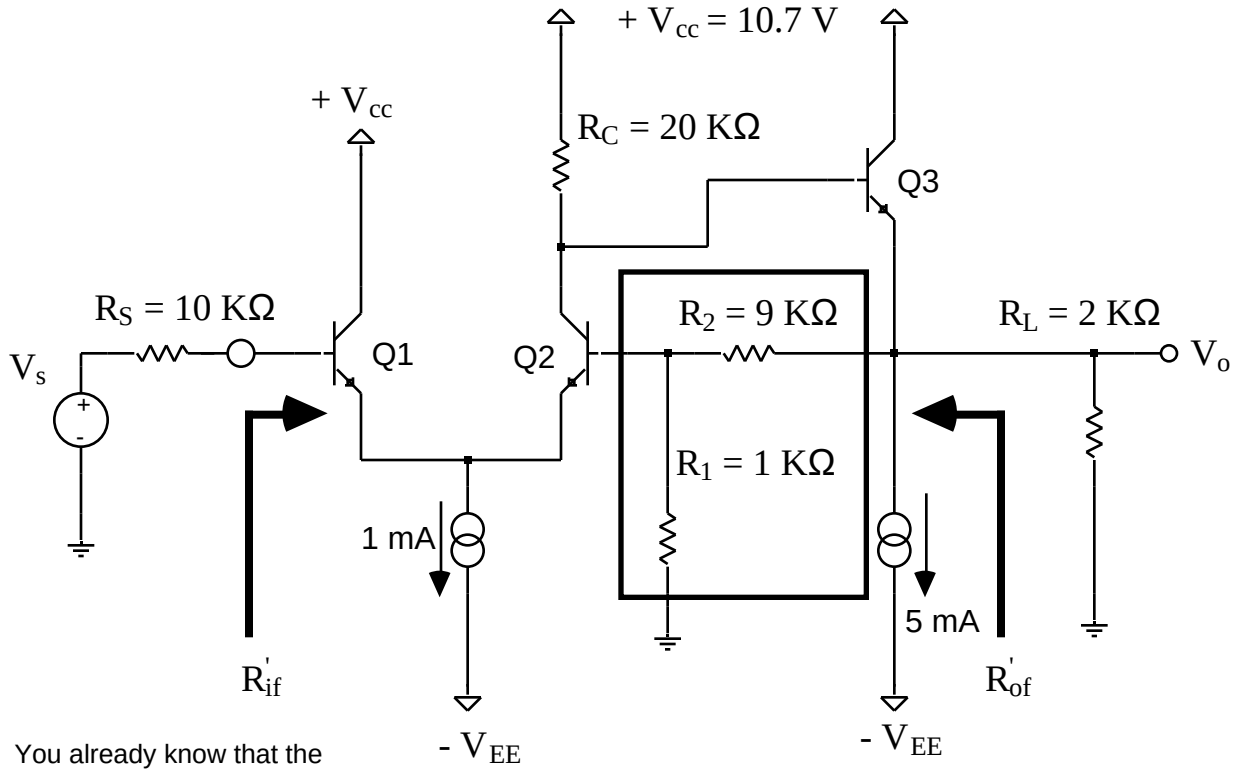
SHORT the SHUNT

$$\beta \equiv \left.\frac{V_f'}{V_o'}\right|_{I_1 = 0}$$

Here we just want "pure" feedback (no worrying about loading anymore)



LET'S TRY IT!!!! SEDRA & SMITH EXERCISE 8.5



You already know that the output voltage of the differential pair is the difference between the inputs!!! As connected, Q2 is the inverting input!

SERIES MIXING **SHUNT SAMPLING**

• First look at the overall design...

• This is a differential amplifier feeding an emitter follower stage at the output.

• Q_1's collector is tied directly to V_{CC} (no collector resistor) to eliminate its Miller capacitance multiplication.

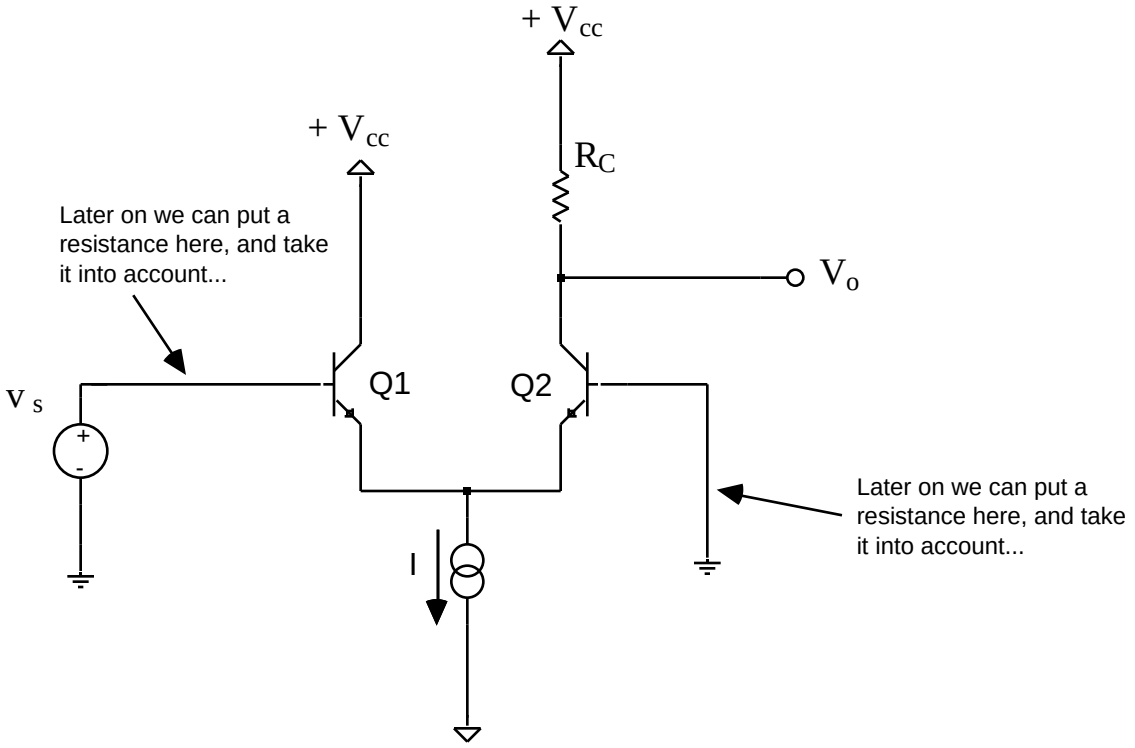
• Look at the circuit and convince yourself that it is really SERIES-SHUNT feedback...

(You were supposed to read section 7.11 before... If you haven't, please do so...)

• DC Voltages.... (β = 100 for all three transistors)

$I_{E1} = I_{E2} = 0.5$ mA

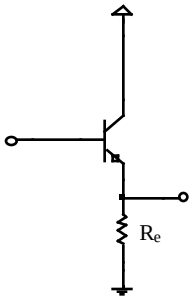
$V_{C2} \approx 10.7 - 0.5$ mA X 20 KΩ = + 0.7 V -> $V_o = 0.7 - V_{BE3} \approx 0$ V



• For the modified (no collector resistor on Q1) differential pair (shown above in simplified form), the voltage gain (to the collector of Q_2) can be quickly determined...

• The circuit is basically a common collector stage driving a common base stage!

• For the common collector stage, we know that the output voltage (at the emitter) is given by,



$$v_e = v_b \frac{R_e}{R_e + r_e}$$

where R_e is the total resistance in the emitter circuit (effectively the **load** of the CC amplifier!) and r_e is the emitter resistance of the transistor in the CC amplifier...

• In this case, $R_e = r_{e2}$, the emitter resistance of Q_2... Therefore, the voltage feeding into the common base stage is just split in half (surprise, surprise!!!),

$$v_{e1} = v_s \frac{r_{e2}}{r_{e2} + r_{e1}} = \frac{v_s}{2} \qquad \text{since} \quad r_{e2} = r_{e1}$$

• The current into the emitter of Q_2 is,

$$i_{e2} = \frac{v_{e1}}{r_e} = \left(\frac{v_s}{2}\right)\left(\frac{1}{r_e}\right) = \frac{v_s}{2r_e}$$

• Therefore, the collector current of Q_2 is,

$$i_{c2} = \alpha \frac{v_s}{2r_e} \approx \frac{v_s}{2r_e}$$

• Finally giving a voltage gain of,

$$A = \frac{v_{C2}}{v_s} = \frac{i_{c2} R_C}{v_s} = \frac{R_C}{2r_e}$$

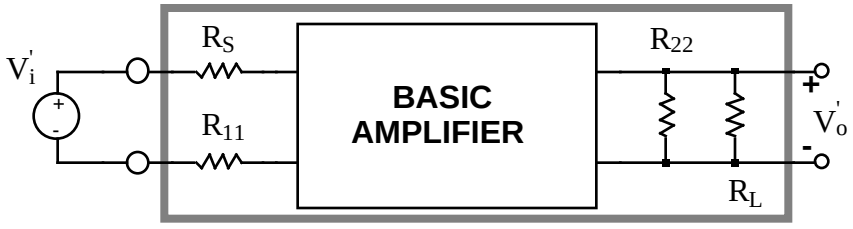
• If we load the input stage with an output stage (Q_3) we need to include that load resistance into a "new" R_C...

• We also know that the input resistance of the CC amplifier is large,

$$R_{iCC} = r_\pi + (\beta + 1) R_e$$

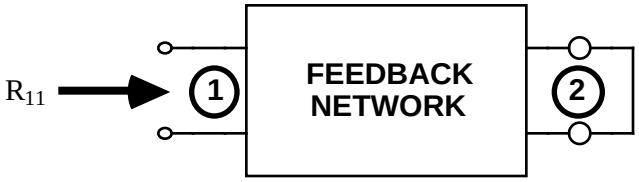
• But in this case it is only about 10 kΩ, so later on we will take into account the effects of R_S... (you may more frequently see a smaller R_S anyway...)

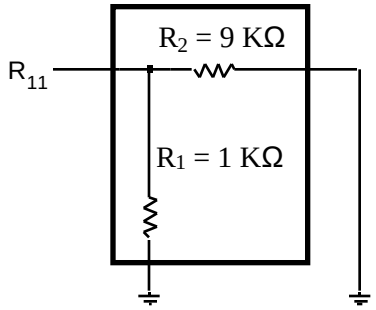
NOW APPLY THE SERIES-SHUNT RULES TO FIND THE "A" CIRCUIT:



• Again, this is the amplifier with all loading effects "lumped" into it.

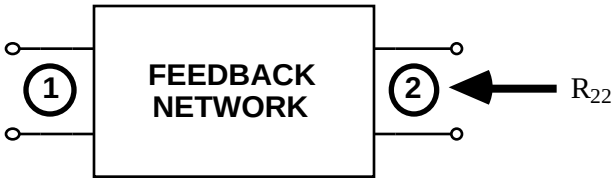
1) Input loading -> **short the shunt** at the output and determine the resistance seen looking into the **INPUT** side of the feedback network...

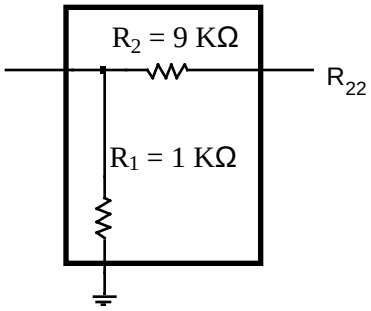




$$R_{11} = 1K\Omega \parallel 9K\Omega$$

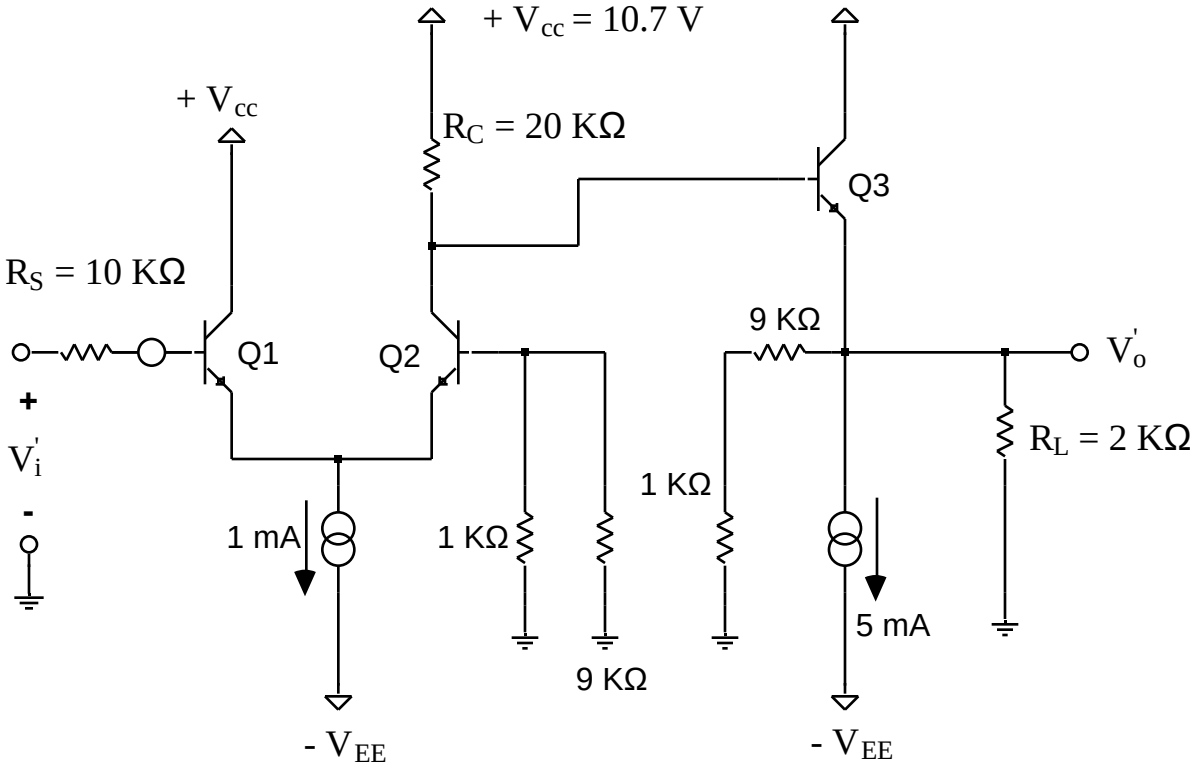
2) Output loading -> **open circuit (sever) the series connection** at the input and determine the resistance seen looking into the **OUTPUT** side of the feedback network....





$$R_{22} = 1K\Omega + 9K\Omega$$

3) Draw the "A" circuit and determine its gain....



• Modifying our previously determined gain equations to take into account the base resistance of Q_2 and the loading of Q_3,

$$A' = \frac{V_o'}{V_i'} = \frac{R_C \parallel (\text{loading from } Q_3 \text{ circuit})}{r_{e1} + r_{e2} + (\text{other loading in the CC emitter circuit})}$$ (Gain of the Q_3 stage)

this stuff is the load on the CC amplifier formed by Q1....

• Plugging it all together and using (β + 1) scaling where necessary,

$$A' = \frac{V_o'}{V_i'} = \left(\frac{R_C \parallel \left[r_{\pi 3} + (\beta_3 + 1)\left([1K\Omega + 9K\Omega] \parallel R_L \right) \right]}{r_{e1} + r_{e2} + \frac{R_S}{(\beta_1 + 1)} + \frac{1K\Omega \parallel 9K\Omega}{(\beta_2 + 1)}} \right) \left(\frac{([1K\Omega + 9K\Omega] \parallel R_L)}{([1K\Omega + 9K\Omega] \parallel R_L) + r_{e3}} \right)$$

• Using the values for r_π and r_e of,

$$r_\pi = \frac{\beta}{g_m} = \frac{\beta V_T}{I_C} \qquad \text{->} \quad r_{\pi 3} \approx 520\ \Omega$$

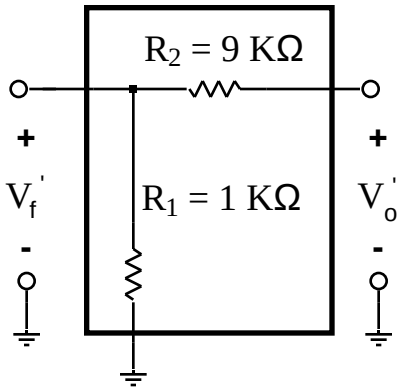
$$r_{e1} = r_{e2} = \frac{V_T}{I_C} \approx 52\ \Omega$$

$$r_{e3} = \frac{V_T}{I_{C3}} \approx 5.2\ \Omega$$

• The result is,

$$A' = \frac{V_o'}{V_i'} = (84.4)(0.997) = 84.1$$

4) Now find the "β" circuit.... (simple voltage divider)



$$\beta \equiv \frac{V_f'}{V_o'} = \frac{R_1}{R_1 + R_2} = \frac{1\ K\Omega}{1\ K\Omega + 9\ K\Omega} = 0.1$$

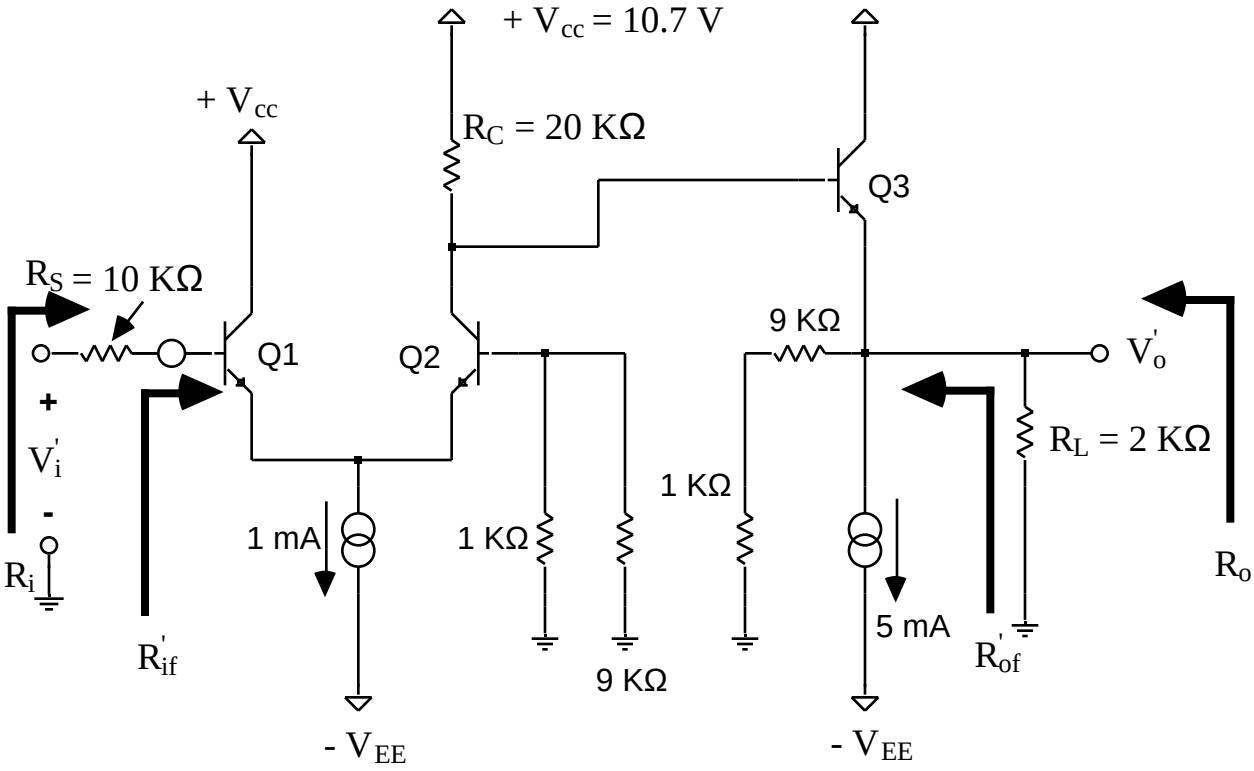
4) Compute the closed-loop gain...

$$A_f = \frac{V_o'}{V_s'} = \frac{A'}{1 + A'\beta} = \frac{84.1}{1 + (84.1)(0.1)} = 8.94$$

• Compare this to the "ideal" non-inverting op-amp configuration... the gain would be,

$$A_V = \left(1 + \frac{R_f}{R_g}\right) = \left(1 + \frac{9k\Omega}{1k\Omega}\right) = 10$$

5) To get the input and output resistances, you need to compute them for the "A" circuit and then apply the feedback equations that you know for the series-shunt case... KEY: you FIRST have to take into account loading and go through the feedback stuff to compute the input and output resistances!



$$R_i = 10\ K\Omega + r_{\pi 1} + (\beta_1 + 1)\, r_{e2} + (\beta_1 + 1)\left[\frac{1\ K\Omega \parallel 9\ K\Omega}{(\beta_2 + 1)}\right]$$

looking at Q2's emitter resistance through the base of Q1

looking at the 1KΩ || 9KΩ resistance through the base of Q1 and through the emitter of Q2

• Which gives (after computing that $r_{\pi 1} \approx 5.2\ k\Omega$) ,

$$R_i = 10\ K\Omega + 5.2\ K\Omega + (101)\,52 + (101)\left[\frac{1\ K\Omega \parallel 9\ K\Omega}{101}\right] = 21.4\ K\Omega$$

• Applying the appropriate feedback equation,

$$R_{if} = R_i\,(1 + A'\beta) = (21.4\ K\Omega)(9.41) = 201\ K\Omega$$

• The actual input resistance of the amplifier (after R_S) can be determined by subtracting R_S...

$$R'_{if} = R_{if} - R_S = 201\ K\Omega - 10\ K\Omega = 191\ K\Omega$$

• Similarly, we start with the output resistance of the "A" circuit,

$$R_o = R_L \parallel (1\ K\Omega + 9\ K\Omega) \parallel \left[r_{e3} + \frac{R_C}{(\beta_3 + 1)} \right]$$

looking at Rc through the emitter of Q3...

which gives,

$$R_o = 2\ K\Omega \parallel (1\ K\Omega + 9\ K\Omega) \parallel \left[5.2\ \Omega + \frac{20\ K\Omega}{(101)} \right] = 181\ \Omega$$

• Applying the appropriate feedback equation,

$$R_{of} = \frac{R_o}{1 + A\beta} = \frac{181\ \Omega}{9.41} = 19.24\ \Omega$$

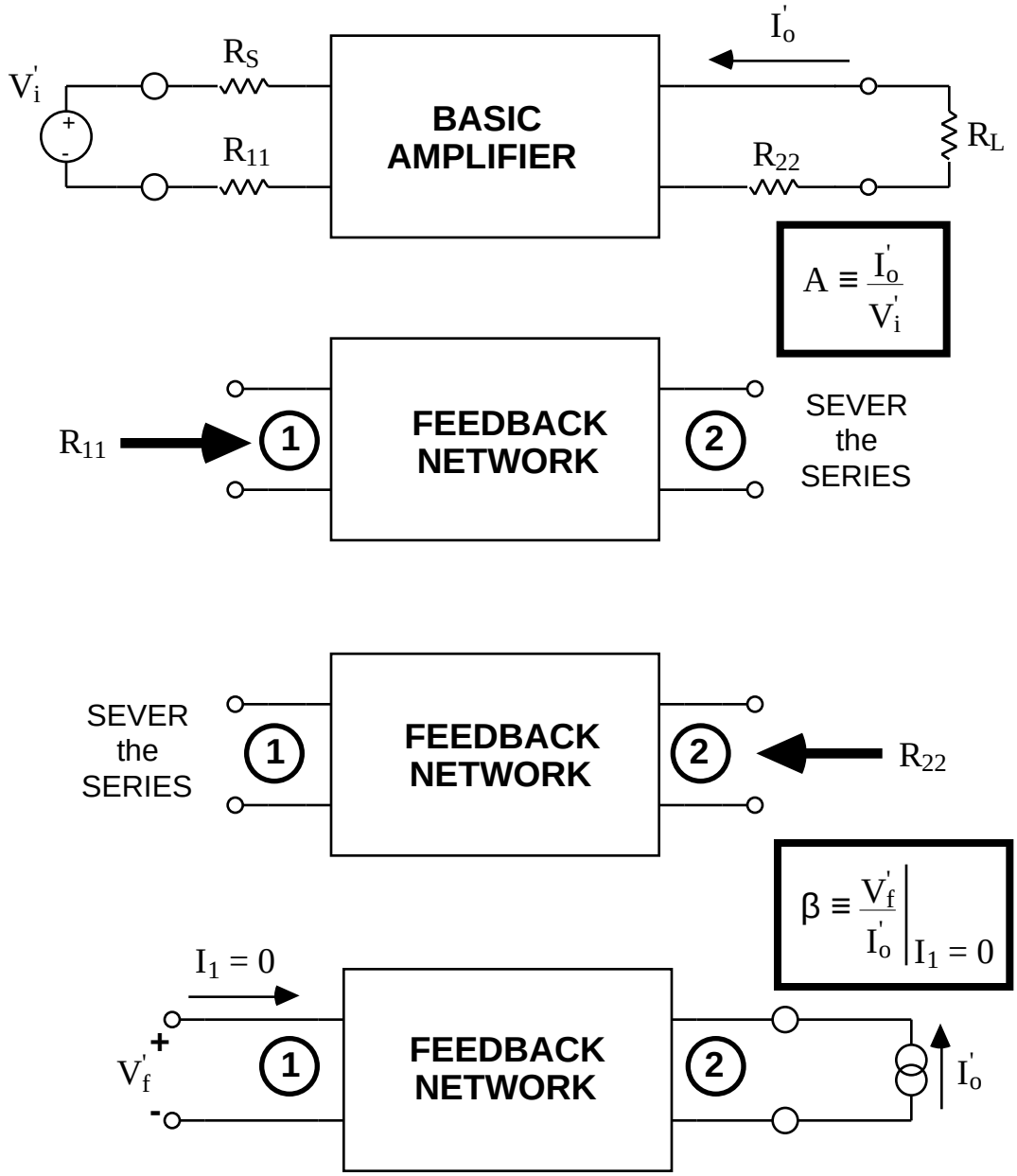
• Finally, to get the **output resistance** of the amplifier ALONE (R_{of}'), we need to remove the effects of R_L in parallel with it...

$$\frac{1}{R'_{of}} + \frac{1}{R_L} = \frac{1}{R_{of}} \qquad \rightarrow \qquad R'_{of} = \frac{1}{\frac{1}{R_{of}} - \frac{1}{R_L}}$$

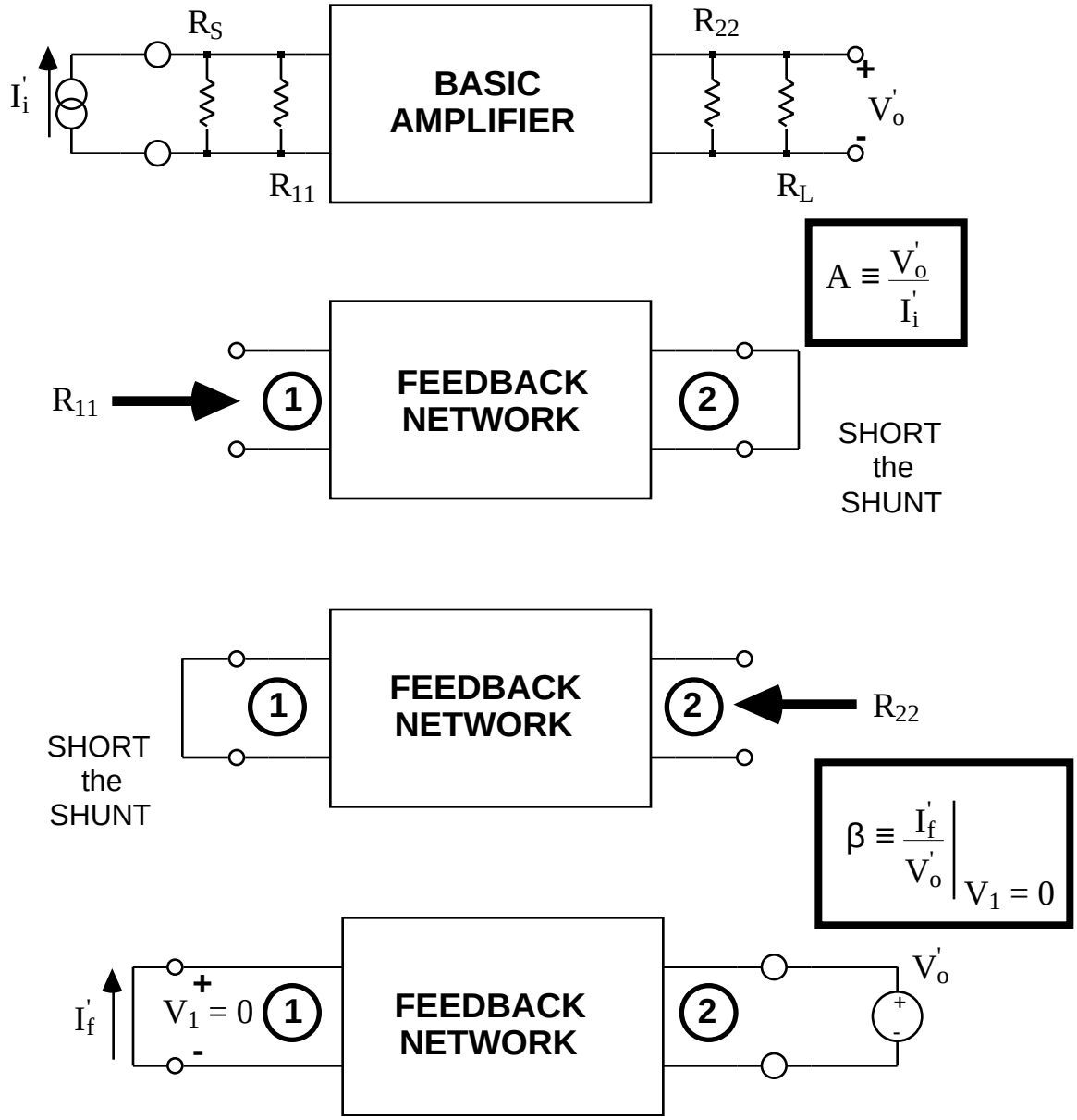
• This gives,

$$R'_{of} = \frac{1}{\frac{1}{19.24\ \Omega} - \frac{1}{2\ K\Omega}} = 19.42\ \Omega$$

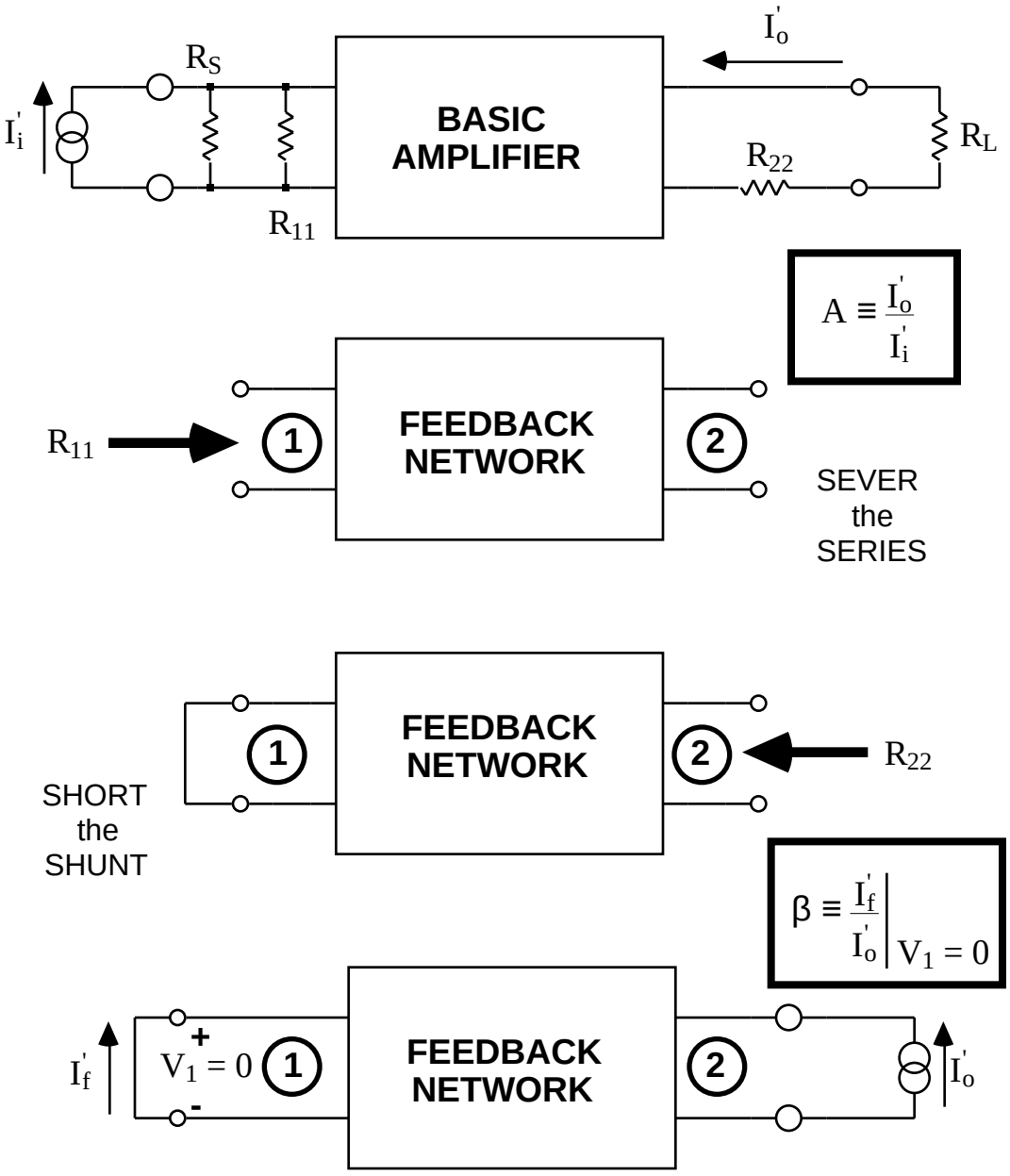
11: RULES FOR SERIES-SERIES (TRANSCONDUCTANCE AMPLIFIER)



12: RULES FOR SHUNT-SHUNT (TRANSRESISTANCE AMPLIFIER)

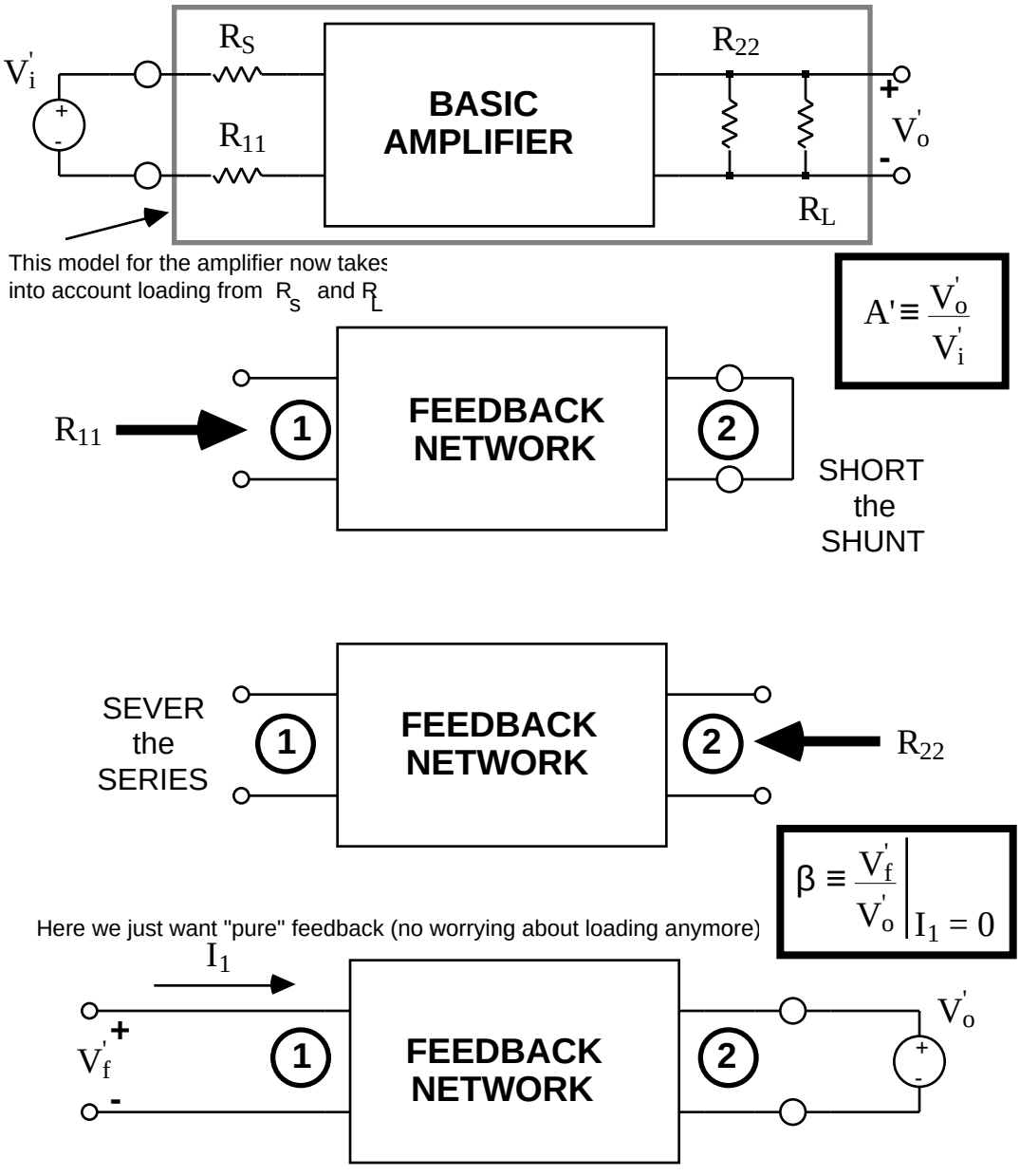


13: RULES FOR SHUNT-SERIES (CURRENT AMPLIFIER)



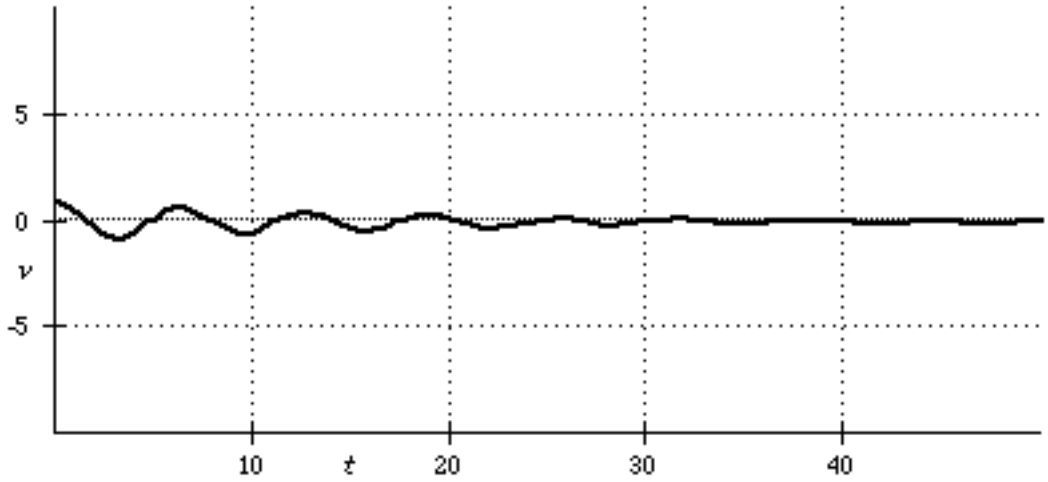
14: RULES FOR SERIES-SHUNT (VOLTAGE AMPLIFIER)

(repeated for convenience)

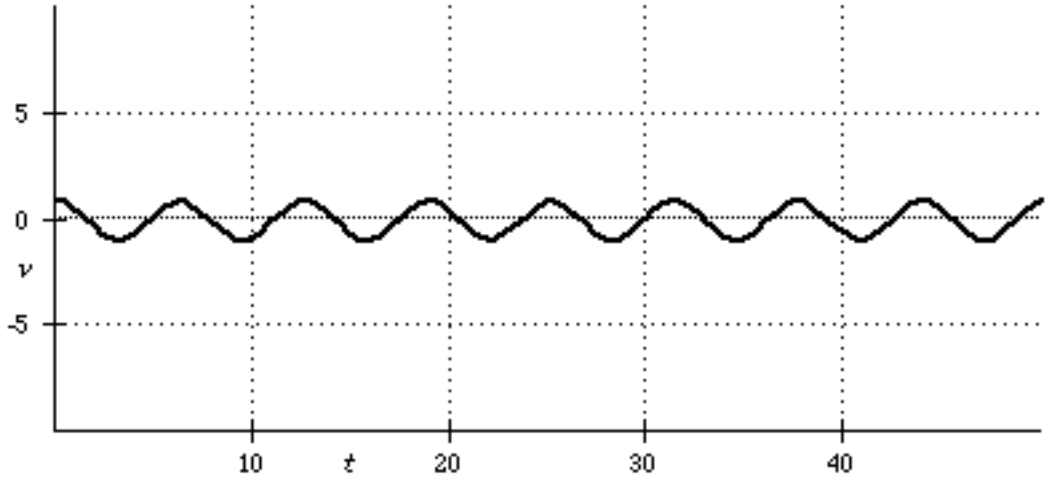


15: STABILITY AND POLE LOCATION

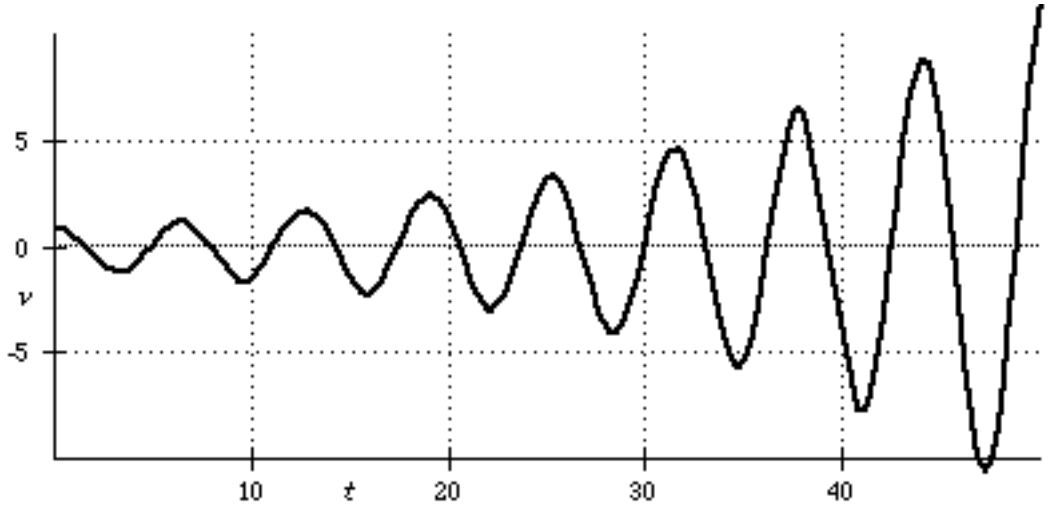
σ = -0.05 Damped oscillations.



σ = 0 An oscillator.



σ = +0.05 Positive feedback out of control!



15.1 SINGLE POLE WITH FEEDBACK

• Remember the response of a single-pole feedback amplifier that we previously looked at can be derived from the response of the amplifier without feedback, given by,

$$A(s) = \frac{A_M}{1 + \frac{s}{\omega_H}}$$

(Sedra & Smith use A_M in section 8.2 and Ao in section 8.9 -> $A_M = A_o$ for a DC-coupled amplifier.)

• If you use the amplifier with negative feedback, the gain becomes,

$$A_f(s) = \frac{A(s)}{1 + \beta A(s)}$$

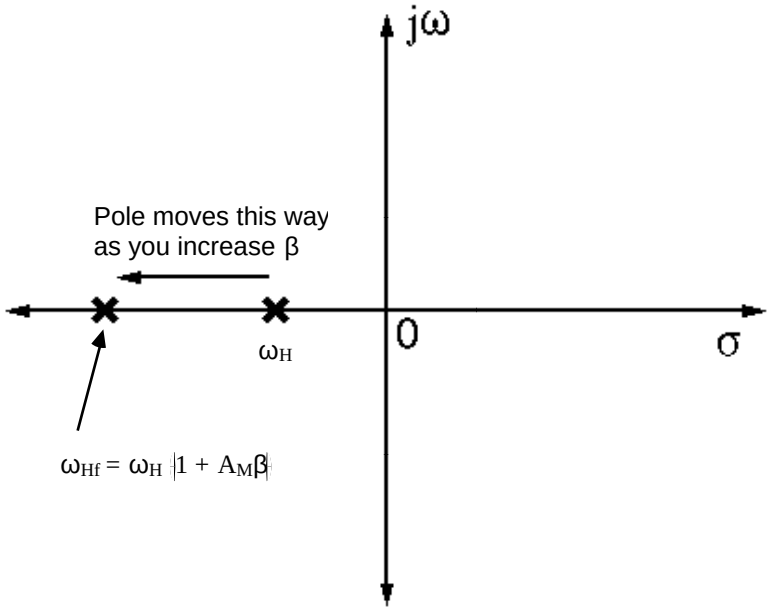
• Substituting, you get,

$$A_f(s) = \frac{\frac{A_M}{(1 + A_M\beta)}}{1 + \frac{s}{\omega_H(1 + A_M\beta)}} = \frac{\text{DC gain}}{1 + \frac{s}{\text{Cut-Off frequency}}}$$

• Thus we have another single-pole response, but with a high cut-off frequency given by,

$$\omega_{Hf} = \omega_H(1 + A_M\beta)$$

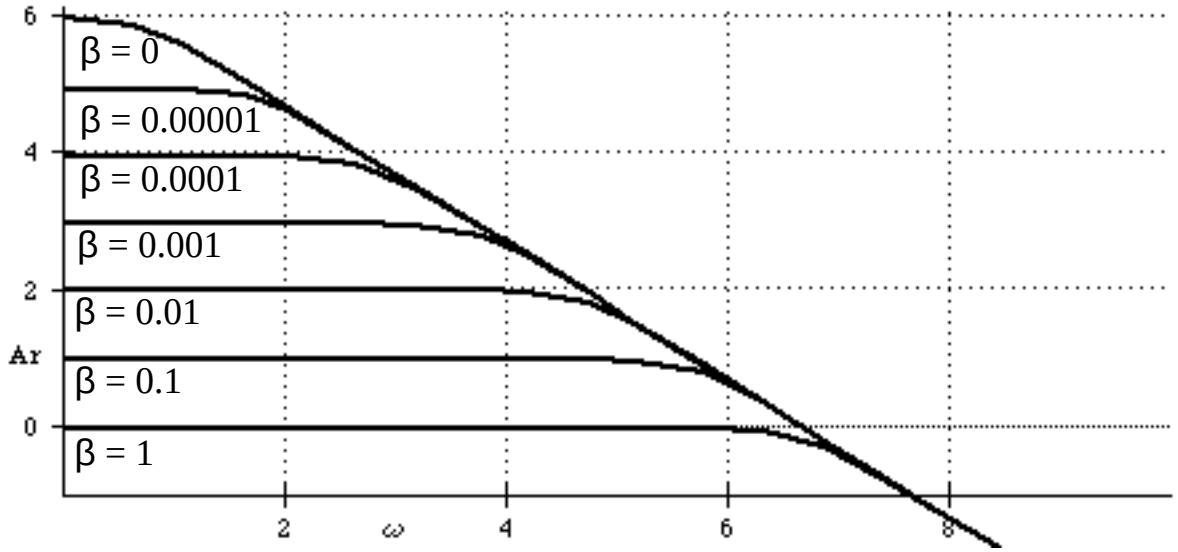
• This means that the pole is sliding along the real axis from its original distance (frequency) ω_H to its new one, ω_{Hf} ....



NOTE that the new pole is given by $0 = 1 + A(S)\beta(S)$.

• ***"Single pole" op-amps are always stable, but real op-amps always have more than one pole!***

• Meanwhile, the frequency response is changing in accord with the gain-bandwidth product....



15.2 TWO POLES WITH FEEDBACK

• For a two-pole basic amplifier, its frequency response can be written as,

$$A(S) = \frac{A_M}{\left(1 + \frac{S}{\omega_{p1}}\right)\left(1 + \frac{S}{\omega_{p2}}\right)}$$

• The closed-loop poles are obtained from $0 = 1 + A(S)\,\beta(S)$, which can be written,

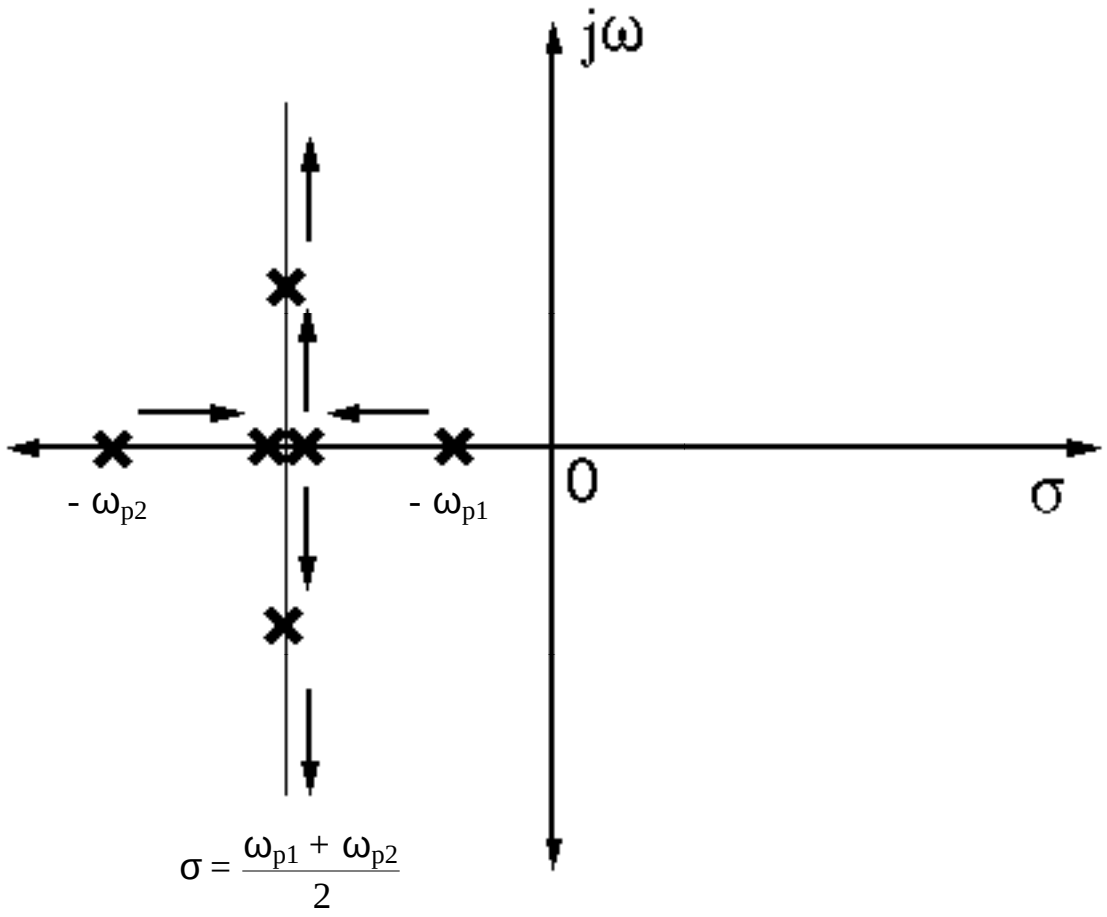
$$S^2 + S(\omega_{p1} + \omega_{p2}) + (1 + A_M\beta)\,\omega_{p1}\,\omega_{p2} = 0$$

• With the closed-loop poles given by,

$$S = -\frac{1}{2}(\omega_{p1} + \omega_{p2}) \pm \frac{1}{2}\sqrt{(\omega_{p1} + \omega_{p2})^2 - 4(1 + A_M\beta)\,\omega_{p1}\,\omega_{p2}}$$

• As ß is increased, the two poles move together on the S-plane until they overlap, and then they separate along a line,

$$\sigma = \frac{\omega_{p1} + \omega_{p2}}{2}$$

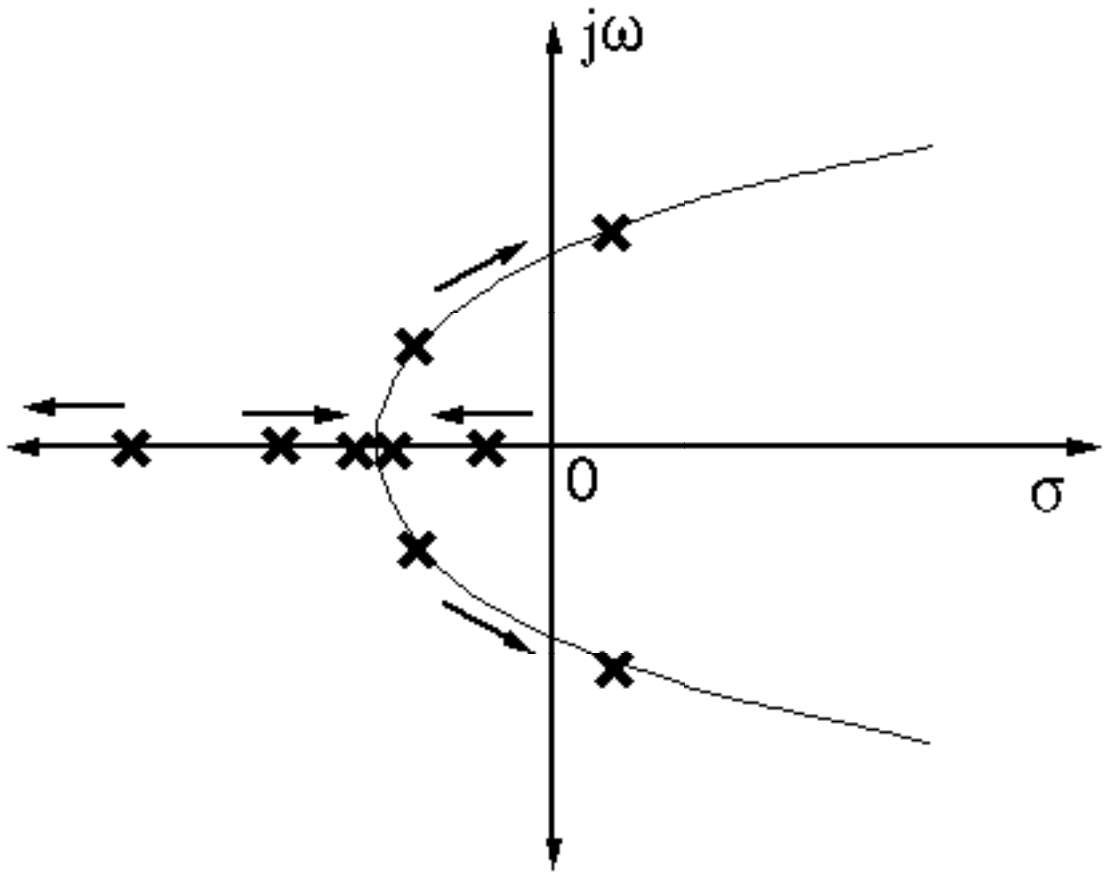


• For a second-order system such as this, the poles never enter the right half-plane (the maximum phase shift is 180°, but it is not reached until $\omega = \infty$).

• So, such an amplifier is **UNCONDITIONALLY** STABLE!

15.3 THREE OR MORE POLES WITH FEEDBACK

• For a basic amplifier with three poles, there is always some value of Aβ that makes a pair of poles enter the RHP! This makes sense for any number of poles greater than two since there is a phase shift of at least 270 °, so that 180° is reached at a finite frequency....



• Two of the poles become coincident, complex and conjugate.

• There is a value of β at which these two poles enter the right half-plane, causing the amplifier to become unstable.

• Because there is a value of β for which the amplifier becomes unstable, one can look at it as a maximum value of β or a minimum gain that guarantees stability.

15.4 STABILITY

• Loop gain = Aβ is a function of frequency...

• Look at the basic feedback equation,

$$A_f(s) = \frac{A(s)}{1 + \beta A(s)}$$

• If | Aβ | > 1 (i.e. there is still some **GAIN** left) when – Aβ = - 180° the feedback will become **POSITIVE**!!!

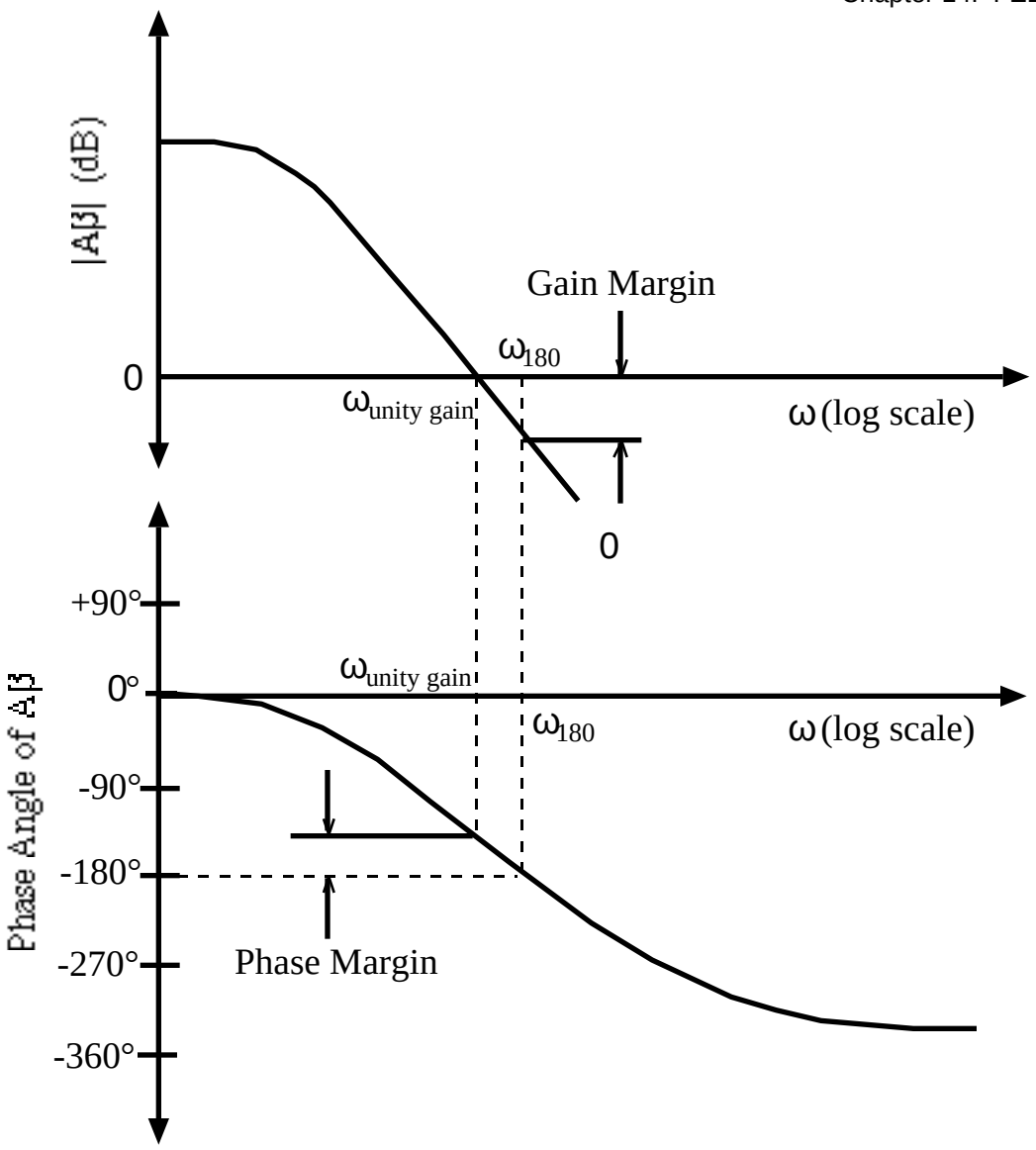
• This leads to instability (i.e. oscillation).

• **Gain Margin** is defined as the difference between the value of | Aβ | at the 180° phase frequency (ω_{180}) and unity....

> Gain Margin ≡ gain at ω_{180} - gain at $\omega_{\text{unity gain}}$ = gain at ω_{180} - 1

• **Phase Margin** is defined as the difference between the phase angle at the unity-gain frequency and at the frequency where the phase reaches 180°...

> Phase Margin ≡ phase at ω_{180} + phase at $\omega_{\text{unity gain}}$ = 180 + phase at $\omega_{\text{unity gain}}$
>
> a negative number usually!



(Figure adapted from A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, HRW Saunders, 1991)

16: COMPENSATION

• Real op-amps have an open-loop gain roll-off with frequency that is approximately first-order (-20 dB/decade) over much of their useful bandwidth.

• The major internal capacitance that causes this roll-off is often referred to as the "dominant pole" of the amplifier.

• At higher and higher frequencies, other capacitance effects come into play as additional poles (sometimes there are three or more).

• This means that the open-loop phase response of the amplifier will eventually reach -90° times the number of poles....

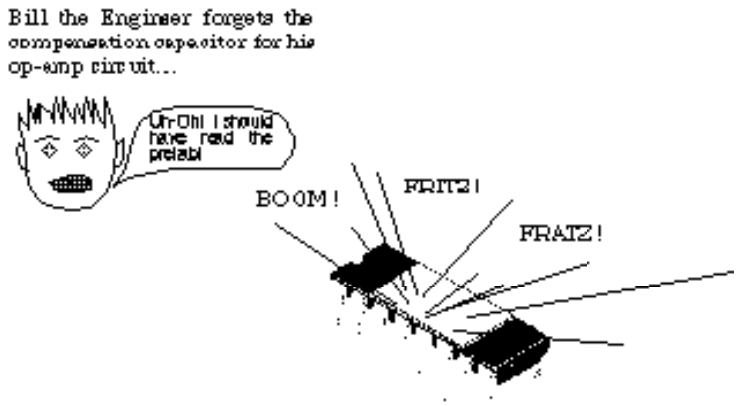
• If the phase is less than -180° when the gain of the amplifier reaches a gain of unity (0 dB), everything remains stable.

• However, if the phase crosses -180° before the gain falls to unity, oscillations will probably occur (since an inverted replica of the amplifier's output is fed back into it)! If an op-amp circuit is unstable, almost any noise present in the circuit will have enough of a high-frequency component to cause the circuit to oscillate.

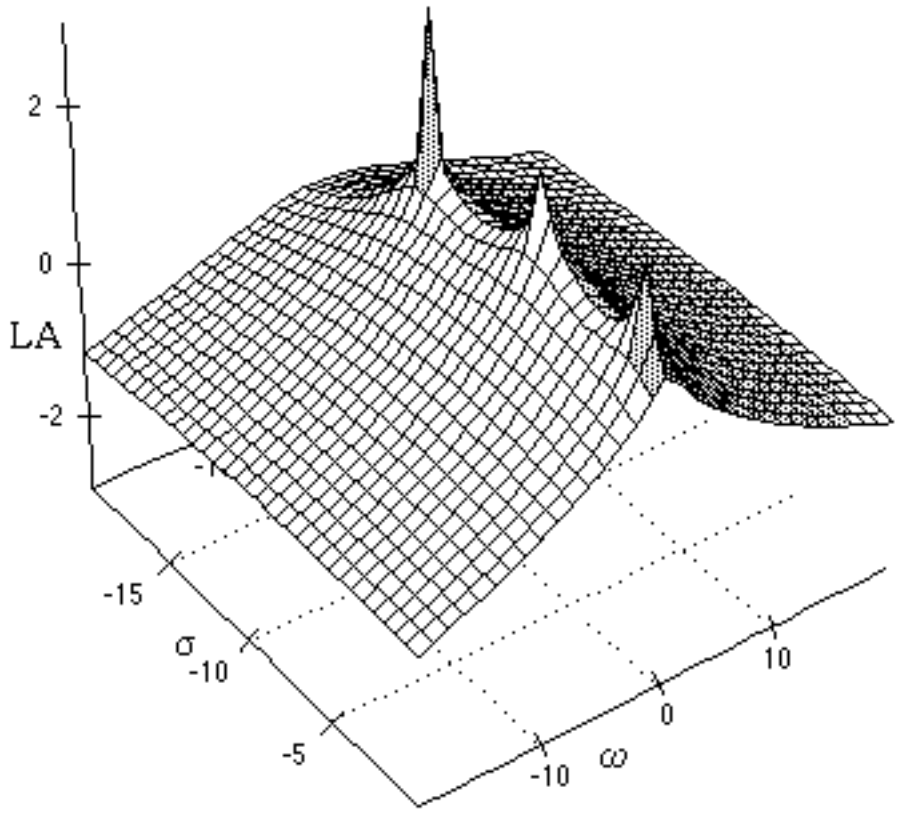
• If the phase crosses -180° at a frequency where the gain of the amplifier is less than unity, the amplifier is "unconditionally stable!"

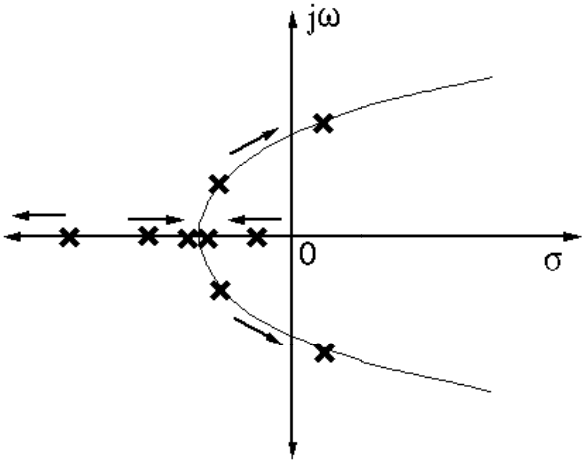
• The most common way to guarantee stability is to compensate the amplifier with some additional components that shape its frequency response so that its gain is less than unity by the time the phase hits -180°. This does, however, compromise the high-frequency response of the amplifier!

• Most op-amps available are "internally compensated," which means that the component(s) required to **guarantee stability** are included **on the chip itself**. Some of the older op-amps, and those designed for high-speed operation, are "externally compensated," which means that you, the designer, must choose external components to assure that the amplifier will not become unstable.



17: "TENT" MODEL FOR VISUALIZING POLES AND ZEROS





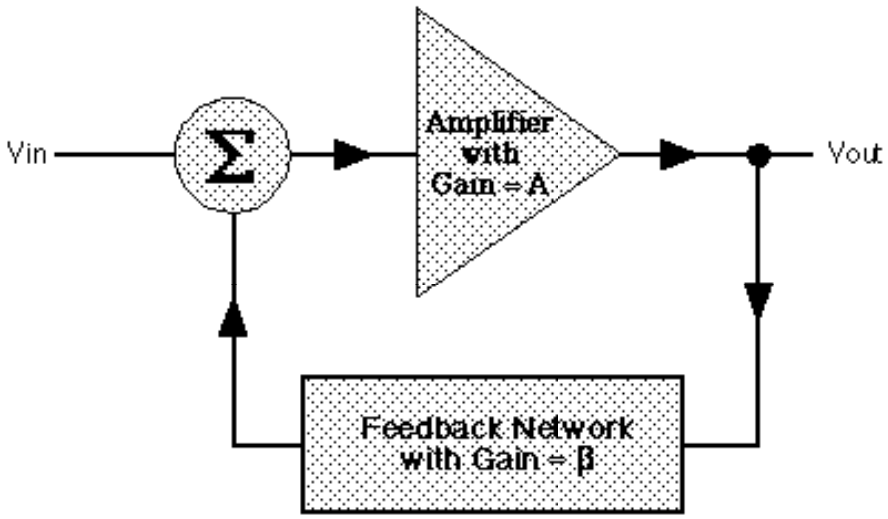
18: LINEAR OSCILLATORS (VERY BRIEFLY!)

• A linear oscillator ideally produces a pure sinusoidal output at a single frequency (hopefully).

• To achieve linear oscillation, a linear amplifier must oscillate without external stimuli (other than a start-up transient to get it going, perhaps).

• In order to understand this type of oscillator, a minor excursion into theory will be required (it's worth it, since a little bit of intuitive understanding goes a long way!).

• What is required to make a linear oscillator (that works, that is!) is the arrangement shown below (this is just **POSITIVE** feedback)...



• A linear oscillator of gain A provides an output voltage v_{out} that is fed through a feedback loop with gain β, and summed back into the input of the amplifier. The overall gain of the circuit with feedback, $A_f(S)$, is given by,

$$A_f(S) = \frac{A(S)}{1 - A(S)\beta(S)}$$

• Without going into all of the details, but by examining the denominator of the above equation, it is easy to see that the overall gain can be made infinity by setting the "round-trip" gain around the entire feedback loop so that,

$$-A(S)\beta(S) = 1$$

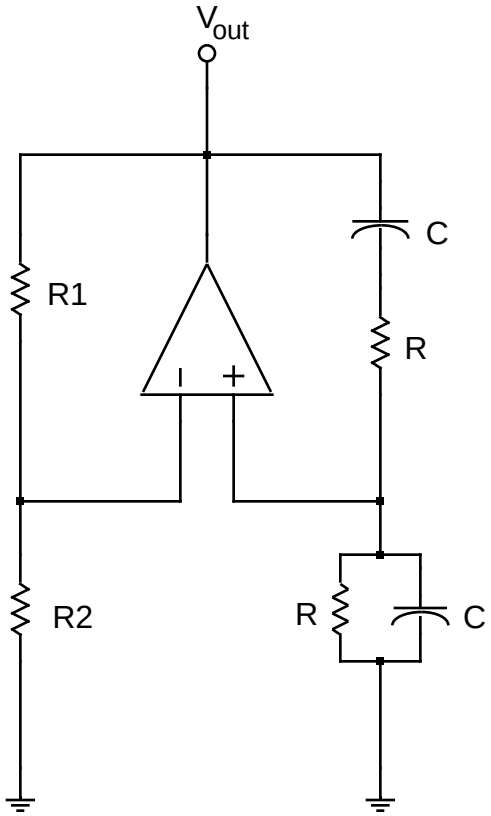
• This condition, known to those who care as the ***Barkhausen Criterion*****,** appears to make the circuit blow up!

• Actually, it is a necessary condition for this type of oscillator (linear) to work.

• Intuitively, however the fact that the overall gain is infinity means that the output of the circuit is some signal (to be determined!), even with NO input at all!

• If one can arrange it so that the Barkhausen Criterion is met at only a single frequency, it is possible to obtain a very pure sinewave output (if it is met at multiple frequencies, you might get an interesting mix of frequencies).

• The classic **Wein Bridge Oscillator** achieves this through a **combination of negative and positive feedback...**



• The oscillation frequency is given by,

$$f_{osc} = \frac{1}{2\pi RC}$$

• The details of the circuit (i.e. actually getting it to start oscillating, keeping it stable, etc.) are covered in EE122 and many good EE reference books...