Lista III – EN2602 Prof Marcelo Perotoni, cap 7 e 8
OBS- Nos circuitos, desenhe sempre o modelo de pequenos sinais correspondente!!

Cap 7

1. (a) What is the expected amplification of a BJT transistor amplifier if the dc supply is set to zero volts?
(b) What will happen to the output ac signal if the dc level is insufficient? Sketch the effect on the waveform.
(c) What is the conversion efficiency of an amplifier in which the effective value of the current through a 2.2-kΩ load is 5 mA and the drain on the 18-V dc supply is 3.8 mA?

3. What is the reactance of a 10-μF capacitor at a frequency of 1 kHz? For networks in which the resistor levels are typically in the kilohm range, is it a good assumption to use the short-circuit equivalence for the conditions just described? How about at 100 kHz?

R: 15.92R para 1kHz, para 100kHz 0.1592R

Cap 8

1. For the network of Fig. 8.64:
(a) Determine Z_i and Z_o.
(b) Find A_v and A_i.
(c) Repeat part (a) with r_o = 20 kΩ.
(d) Repeat part (b) with r_o = 20 kΩ.

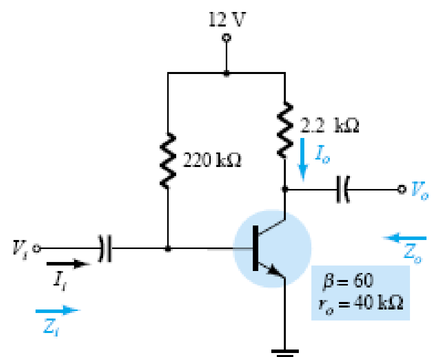


Figure 8.64 Problems 1 and 21

R: (a) Zi=497.5 Zo=2k2 (b) Av=-264.74 Ai=beta (c) Zi o mesmo antes, Zo=1.98K (d) Av=-238.27 e Ai=53.88

2. For the network of Fig. 8.65, determine V_{CC} for a voltage gain of $A_v = -200$.

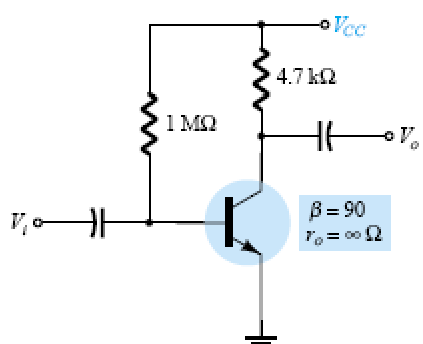


Figure 8.65 Problem 2

R: Vcc=12.85

4. For the network of Fig. 8.67:
(a) Determine r_e.
(b) Calculate Z_i and Z_o.
(c) Find A_v and A_i.
(d) Repeat parts (b) and (c) with $r_o = 25\ \text{k}\Omega$.

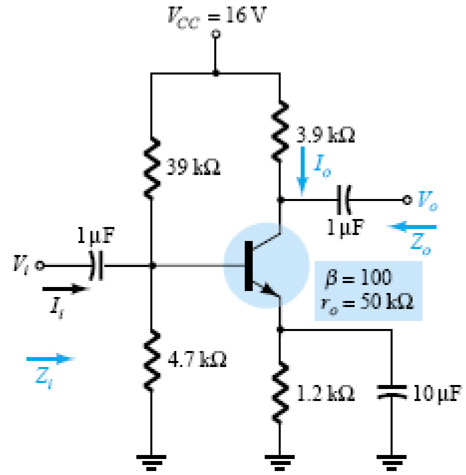


Figure 8.67 Problem 4

R: (a) re=30.56 (b) Zi=1.768k e Zo=3k9 (c) Av=-127.6 Ai=57.85 (d) Av=-110.28 Ai=50

5. Determine V_{CC} for the network of Fig. 8.68 if $A_v = -160$ and $r_o = 100\ \text{k}\Omega$.

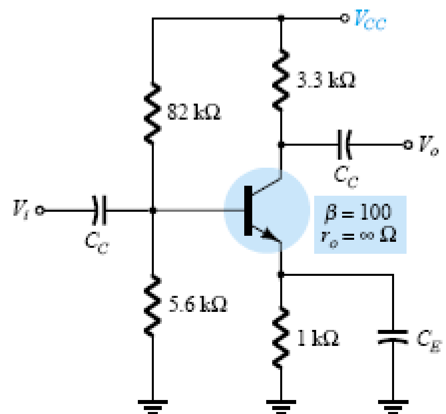


Figure 8.68 Problem 5

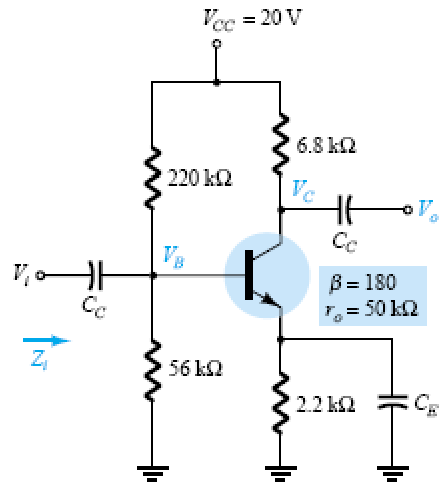
R: Vcc=30.68

6. For the network of Fig. 8.69:

(a) Determine r_e.

(b) Calculate V_B and V_C.

(c) Determine Z_i and $A_v = V_o/V_i$.



R: (a) re=18.95 (b) Vb=3.72 e Vc=10.72 (c) Zi=3.17k e Av=-315.88

7. For the network of Fig. 8.70:

(a) Determine r_e.

(b) Find Z_i and Z_o.

(c) Calculate A_v and A_i.

(d) Repeat parts (b) and (c) with $r_o = 20\ \text{k}\Omega$.

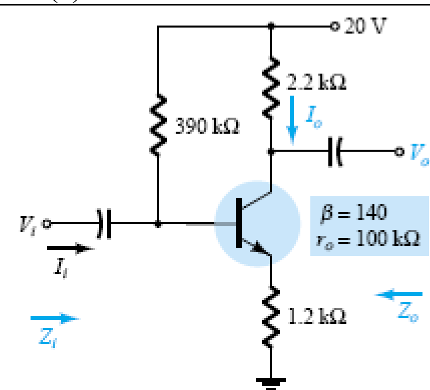


Figure 8.70 Problems 7 and 9

R: (a) re=5.34 (b) Zo=2200 e Zi=118.37 (c) Av=-1.82 (d) Av=-1.81 Ai=87.17

* **10.** For the network of Fig. 8.72:

(a) Determine r_e.

(b) Find Z_i and A_v.

(c) Calculate A_i.

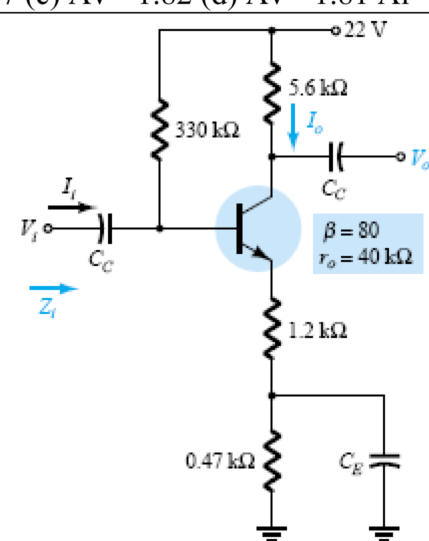


Figure 8.72 Problem 10

R: (a) re=7 (b) Zi=66.82k Av=-4.57 (c) Ai=54.53

11. For the network of Fig. 8.73:

(a) Determine r_e and βr_e.
(b) Find Z_i and Z_o.
(c) Calculate A_v and A_i.

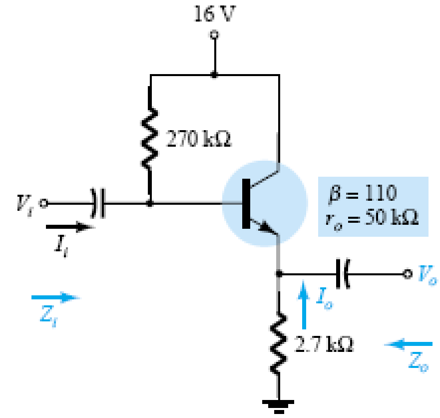


Figure 8.73 Problem 11

(a) re=8.72 (b) Zi=142.25k Zo=8.69 (c) Av=0.997 Ai=-52.3

14. For the common-base configuration of Fig. 8.76:

(a) Determine r_e.
(b) Find Z_i and Z_o.
(c) Calculate A_v and A_i.

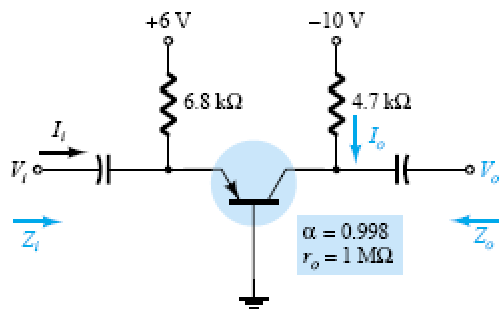


Figure 8.76 Problem 14

(a) re=33.38 (b) Zi=33.22 Zo=4K7 (c) Av=alfa*Re/re=140.52 Ai=-alfa=-0.998

* **15.** For the network of Fig. 8.77, determine A_v and A_i.

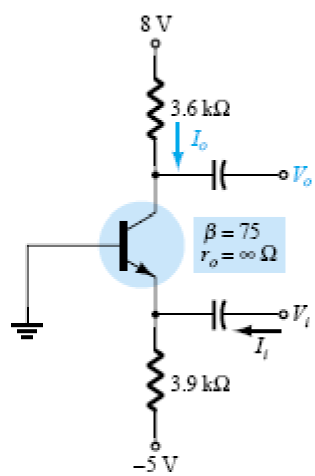


Figure 8.77 Problem 15

R: (a) Av=163.2 Ai=-alfa=-0.968

16. For the collector FB configuration of Fig. 8.78:

(a) Determine r_e.
(b) Find Z_i and Z_o.
(c) Calculate A_v and A_i.

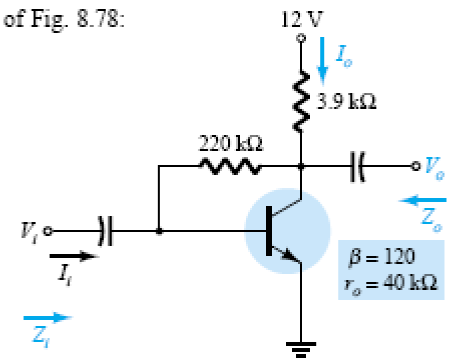


Figure 8.78 Problem 16

R: (a) re=10.08 (b) usa formula aproximada para Zi=498 Zo=3k83 (c) Av=-298 Ai=38.37

Sedra Smith, 5ª edição

D5.56 Consider the CE amplifier circuit of Fig. 5.26(a) when operated with a dc supply $V_{CC} = +5$ V. It is required to find the point at which the transistor should be biased; that is, find the value of V_{CE} so that the output sine-wave signal v_{ce} resulting from an input sine-wave signal v_{be} of 5-mV peak amplitude has the maximum possible magnitude. What is the peak amplitude of the output sine wave and the value of the gain obtained? Assume linear operation around the bias point. (*Hint:* To obtain the maximum possible output amplitude for a given input, you need to bias the transistor as close to the edge of saturation as possible without entering saturation at any time, that is, without v_{CE} decreasing below 0.3 V.)

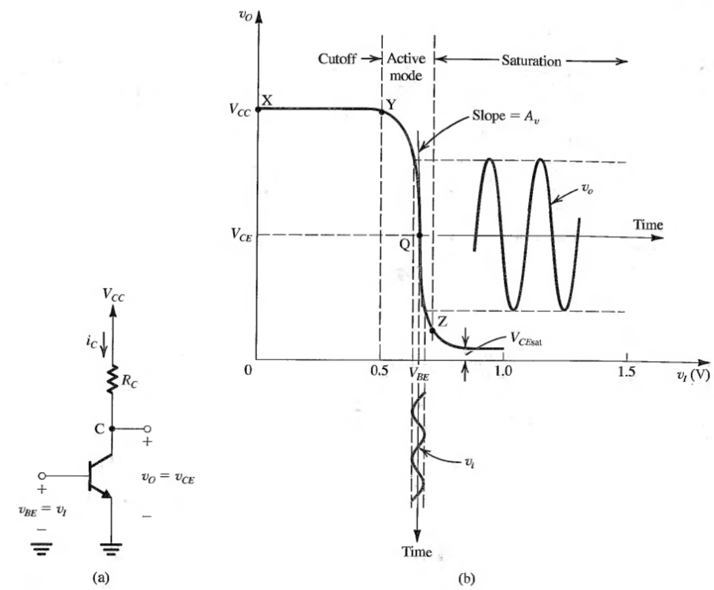


FIGURE 5.26 (a) Basic common-emitter amplifier circuit. (b) Transfer characteristic of the circuit in (a). The amplifier is biased at a point Q, and a small voltage signal v_i is superimposed on the dc bias voltage V_{BE}. The resulting output signal v_o appears superimposed on the dc collector voltage V_{CE}. The amplitude of v_o is larger than that of v_i by the voltage gain A_v.

R: Av=-156.67 **Nota**: V_T para esse autor é 25mV

Dica: Esboce a saida grafica da tensao total no coletor, deve ser uma soma da tensao DC quiescente + ganho, no ponto mais baixo o sinal deve ser maior ou igual a 0.3V. Depois expresse o ganho do emissor comum da figura em funcao de Rc,Ic e Vt e o resultado ira aparecer, considerando a tensao minima como sendo obrigatoriamente 0.3V.

5.57 The transistor in the circuit of Fig. P5.57 is biased at a dc collector current of 0.5 mA. What is the voltage gain? (*Hint:* Use Thévenin theorem to convert the circuit to the form in Fig. 5.26a).

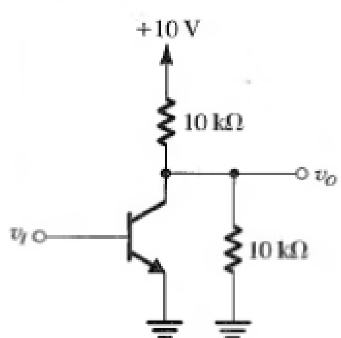


FIGURE P5.57

Dica: por Thevenin, entenda simplesmente o paralelo de Rc com Rl. Use as considerações do exercicio acima e a resposta sai fácil.

R: Av=-100