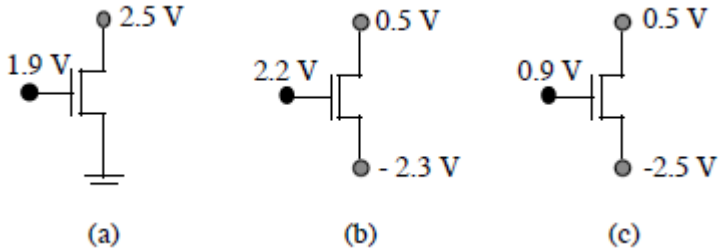
Lista VI EN2719 Prof Marcelo Perotoni

(Introduction to Digital Electronics by Chuck Hawkins and Jaume Segura)

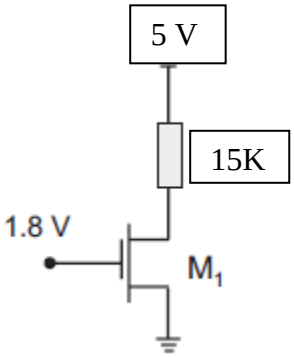
1. Para os transistores NMOS Enhancement abaixo, defina em qual região eles estão operando (triodo, off ou saturação). Considere Vth=0.4 V. Considere o dispositivo saturado se

$$V_{DS} > V_{GS} - V_t$$



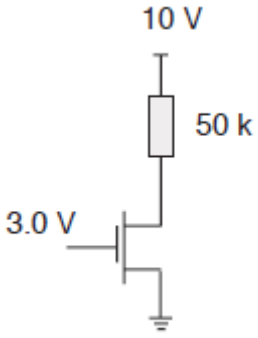
R: (a) Saturado (b) não saturado (região triodo) (c) fronteira entre saturado e triodo

2. Para o circuito NMOS enhancement, considere k=300E-6, Vth=0.6V. Calcule I_D e V_{DS}. DICA: não se sabe, a priori, a condição do dispositivo (saturado ou triodo), assim suponha uma condição e verifique a consistência do resultado.



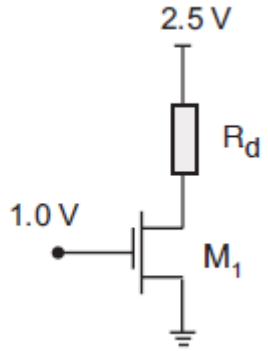
R: V_{DS}=0.53 V e I_{DS}=298 uA

3. Para o circuito NMOS enhancement, considere k=75E-6 A/V^2, Vth=0.5 V. Calcule I_D e V_{DS}. DICA: não se sabe, a priori, a condição do dispositivo (saturado ou triodo), assim suponha uma condição e verifique a consistência do resultado.



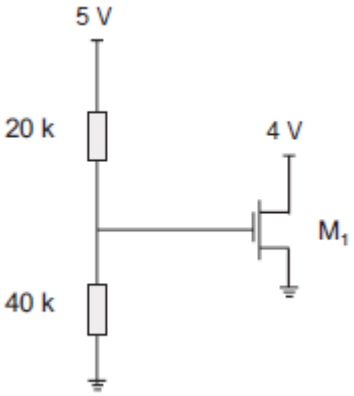
R: V_{DS}=0.56 V e I_{DS}=0.18 mA

4. Calcule o valor de Rd que coloca o NMOS enhancement na região de triodo, considere k=500E-6 A/V^2, Vth=0.4 V.



R: R_D=10.56K

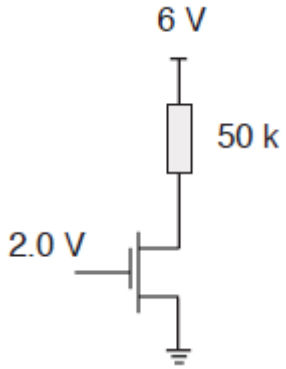
5. Calcule a condição (saturado/triodo/off) do NMOS enhancement abaixo.



Vth=0.5

R: saturado (V_{GS}=3V3)

6. Calcule ID e VD e verifique o status do NMOS enhancement (saturação ou triodo). K= 100 uA/V^2 e Vth=0.5.



R: VDS=0.43 V e IDS=0.11 mA

Boylestead

17. For the self-bias configuration of Fig. 6.81, determine:
(a) I_{DQ} and V_{GSQ}.
(b) V_{DS} and V_D.

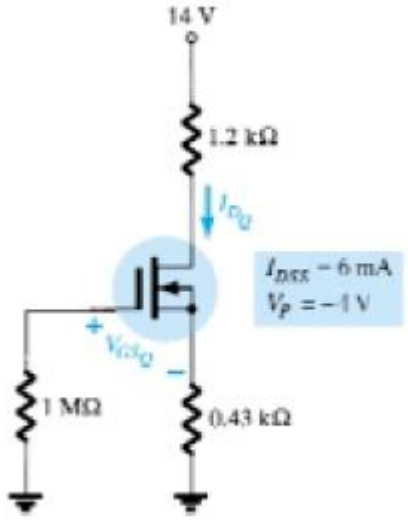


Figure 6.81 Problem 17

Vp= -4V (figura borrada)
R: V_{GS}=-1.2 V e I_D=2.8 mA

* **18.** For the network of Fig. 6.82, determine:
(a) I_{D_Q} and V_{GS_Q}.
(b) V_{DS} and V_S.

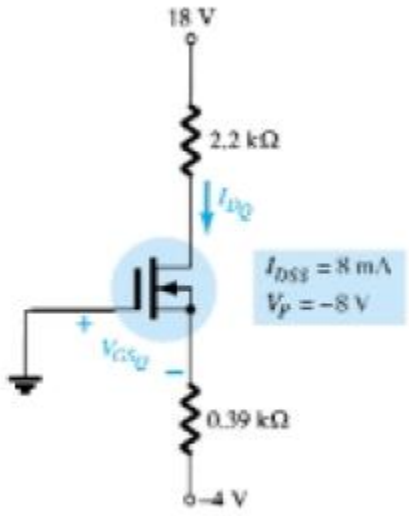


Figure 6.82 Problem 18

R: I_D= 9mA, V_{GS}=0.49V V_{DS}=-1.31 V_S= -0.49

19. For the network of Fig. 6.83, determine:
(a) I_{D_Q}.
(b) V_{GS_Q} and V_{DS_Q}.
(c) V_D and V_S.
(d) V_{DS}.

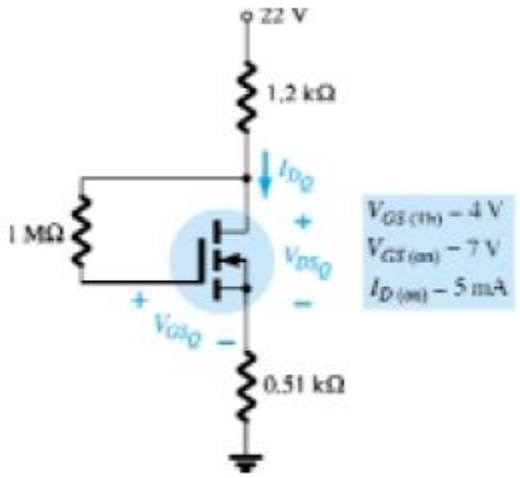


Figure 6.83 Problem 19

Borrado: V_{GSTH}=4 V_{GSON}=7 I_{DSON}= 5 mA
R: I_D= 8mA, V_{GS}=V_{DS}=8.32 V_D= 12.4 e V_S= 4.08

20. For the voltage-divider configuration of Fig. 6.84, determine:
(a) I_{D_Q} and V_{GS_Q}.
(b) V_D and V_S.

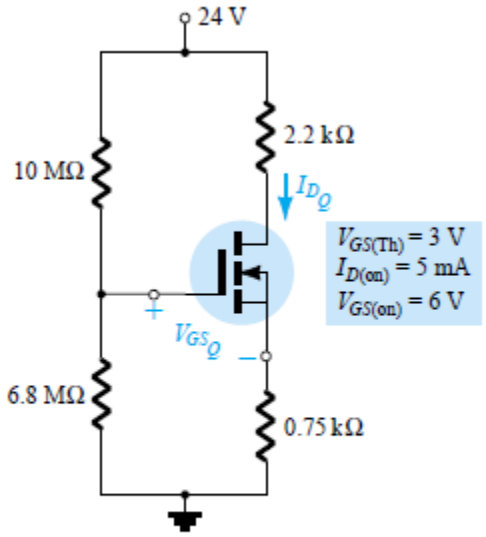
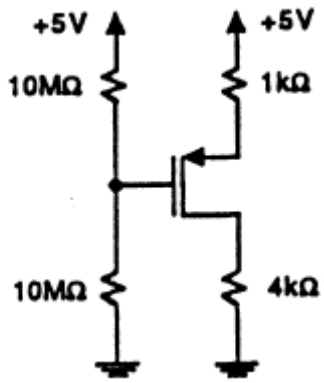


Figure 6.84 Problem 20

R: I_D= 5mA, V_{GS}=5.96V V_D= 13 e V_S= 3.75

Sedra Smith

5.19 Calcule V_D para k=0.5 mA/V2 e VT=1V. P-enhacement MOSFET



R: V_D=2V

Microelectronic Circuit Design, Jaeger, 4th ed

4.34 Para o circuito abaixo ambos transistores tem k=500 uA/V^2, V_{DD}=10V e V_{TH}=0.75 V, enhancement NMOS, calcule I_D.

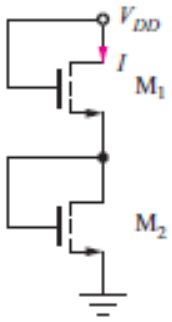


Figure P4.34