Development of Doped Graphene Oxide Resistive Memories for Applications Based on Neuromorphic Computing

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Abstract. Resistive random access memory ReRAM has attracted great attention due to its potential for flash memory replacement in next generation non-volatile memory applications. Among the main characteristics of this type of memory, we have: low energy consumption, high-speed switching, durability, scalability and friendly manufacturing process. This device is based on resistive switching phenomenon for operation, which is reversible and can be played back repeatedly. In this work, eight different devices are developed and fabrication is made as follows: thin films are obtained by dip coating technique. The dip coating apparatus basically consists of a clamp which holds the substrate is dipped in a GO solution (graphene oxide) which containing dopant (cupper, iron or silver) or CuO (copper oxide). ITO (indium tin oxide) and aluminum contacts were evaporated. The devices were developed with purpose: intention is record and read information dynamically with appropriate algorithm. There is even the possibility of storing images. With these functions, it would be promising to enter the neuromorphic computing area that is one of the resistive memory applications. ReRAM technology advent represents a paradigm shift for artificial neural networks, being the best candidate for emulation of synaptic plasticity and learning mode.

Keywords: Resistive memory · ReRAM · Graphene oxide

1 Introduction

Resistive random access memories (ReRAMs) are a class of devices emerging from the new generation of non-volatile memories. Many researchers have made great efforts to understand and develop these new memories because they have simple metal-insulator-metal (MIM) structure [1, 2], ease of recording/reading, high storage density and low power consumption. Resistive switching (RS) is the basic phenomenon for the operation of these memories, in which when a specific electrical voltage is applied in the MIM device, it can undergo switching from its initial insulator resistance state (HRS - high resistance state) to a low resistance state (LRS).

RS has already been observed in several materials such as TiO2, ZnO, NiO, perovskites and some electrolytic solids [1–5], in which two typical behaviors were perceived: unipolar and bipolar. In the unipolar behavior the switching is independent of the polarity applied, whereas in bipolar behavior there is this dependence [4].

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Among the main characteristics of this type of memory, we have: low energy consumption, high-speed switching, durability, scalability and friendly manufacturing process [1].

There is a strong relationship between the materials used in the composition of these devices and their characteristics. Depending on the composition of the insulator, the voltage and current where the LRS and HRS states will occur can vary greatly; The response time for switching from one state to another or latency is affected and the power consumption for which SET and RESET occur are also influenced. The unipolar or bipolar behavior will depend on the type of material chosen. Contacts also have influence on the phenomenon of resistive switching and filament formation, and may interfere with the mode of memory operation. The geometry of the device is another element that causes impact. This makes it necessary to choose an optimized architecture because of the scalability issue.

Graphene is currently one of the most promising nanomaterials in the world, due to its excellent electrical, thermal and optical properties. Graphene is considered to be the basis of the whole family of carbon materials, with the exception of diamond [6–9]. For its production several methods have been researched [10], exemplified by exfoliation, deposition by CVD (Chemical Vapour Deposition) technique, among others.

Thinking in terms of obtaining the devices, process and waste disposal, we have an optimization, since the process of obtaining the memories is simple, low cost and there is no generation of toxic waste. If we think about the production of materials, some techniques are expensive (such as MBE or molecular beam epitaxy) and others end up generating toxic materials (such as the production of silicon oxide that sometimes uses silane gas). Graphene oxide would be a “green” material which does not pollute and is still derived from carbon.

The production process is simple, efficient and inexpensive. It can be done with low-cost equipment that can be build by the researcher. Moreover, due to the simplicity, the reproducibility of the devices can be made on a large scale.

What is the advantage of using a dopant in material? When the material is doped, in case graphene oxide (GO), its electrical, optical, magnetic and structural characteristics are modified. They can be improved or only directed towards a particular purpose. If we are to think in terms of resistive memories, it is necessary to obtain characteristics that allow a greater miniaturization of the devices, since the flash technology reached its lower limit because the minimum thickness of 15 nm has been reached. In addition, it is expected that there will be a minimum energy consumption with respect to the operation of a ReRAM, with SET and RESET voltage values occurring at low voltages.

Heat dissipation must be considered due to the Joule Effect, so it is important to have control over how the memory will operate in unipolar or bipolar mode. If the ReRAM is unipolar, its SET and RESET will occur for the same polarity; being unipolar, we have that there will be no influence of the electric current, thus avoiding the heating of the device with Joule Effect. In Yoo et al. research [13] devices were developed using pure graphene oxide. Memories presented bipolar behavior and the voltage for both RESET and SET are low, besides the variation in the current values are perceptible. When the GO is doped with some transition metal such as iron, copper or silver, the behavior is changed to unipolar and the SET and RESET occur for smaller voltages, saving energy.

The emergence of portable electronics such as cell phones, MP3 s, digital cameras and netbooks over the last 20 years has led to unbridled demand for better technologies for non-volatile flash memory because of its small cell size and low power consumption. However, scaling of flash memory beyond 15-nm technology is highly problematic due to fundamental limit of cell structure. The cell of a flash memory unit is very similar to the conventional field-effect metal-oxide-semiconductor transistor (MOSFET), except for the additional floating port for storing electrical charges.

Research on non-volatile memories to replace the flash has been very active. Among the most recent and as an alternative that has generated promising results, there is resistive memory (ReRAM) that is based on the resistive switching phenomenon (RS). Basically, non-volatile resistive RAM stores data by creating a resistor in a circuit instead of trapping electrons inside a cell. As a result, while the usual memory read-out latency is hundreds of microseconds, ReRAM reaches 50 ns, a delay time that can fit between main memory and cache memory levels in terms of speed, but at a lower cost.

Resistive Switching refers to the physical phenomena through which the resistance of a dielectric undergoes changes in response to a strong external electric field. It differs from degradation phenomena in dielectrics, which result in a permanent reduction in the resistance so that the change back to the original state is no longer possible [11, 12].

RS process is reversible and can be reproduced countless times. Typically, the change in resistance is non-volatile. Note that these phenomena occur in numerous insulating materials, including oxides, nitrides, chalcogen, organic semiconductor materials. However, the RS phenomenon has been studied more extensively in oxides. ReRAM are based on this phenomenon for operation [13–15].

Basically, memristor is an extremely small (nanometer) component that combines two terminals; when a current flows between them, its resistance increases; when the opposite path is made, the resistance decreases. What is important to consider here is that when current is cut off, the last recorded resistance level is maintained and depending on its value, we can assign a logic level 0 or 1.

RS mechanism is still not very well understood and therefore there are some proposals to explain this process. Predominantly more accepted model in oxide structures is the "conductive filament" model. A conductive path is created inside the insulator when certain electrical voltage is applied, the so-called "forming process" or SET. This creation occurs due to ionic migrations inside the insulator. RESET would be the destruction of this filament. The formation/destruction of filament can occur in two ways: one of these migrations is anionic, in which oxygen atoms migrate towards the anode, leaving behind a path of cations. Another ionic migration that occurs inside the insulator is cationic one, in which one of the electrodes is electrochemically active (such as Ag) and the other being an inert material (Pt, for example), and in addition, the insulator must be conductor of cations.

2 Experimental

Copper oxide (CuO) was synthesized using copper (II) acetate as described by Yoo et al. [13]. A colloidal solution of copper acetate in ethanol was used as precursor. 0.3 g copper acetate monohydrate added to 30 mL ethanol was suffered sonication for 1 h. To make CuO thin films, dip coating was used.

Deposition is made as follows: thin films are obtained by dip coating technique. The dip coating apparatus basically consists of a clamp which holds the substrate is dipped in a GO solution (graphene oxide) which containing dopant (cupper, iron or silver) or CuO. ITO (indium tin oxide) and aluminum contacts were evaporated.

The current and voltage relation can be measured by tracer IxV model HP 4140B. A curve is generated by varying the voltage. For the device to be considered a ReRAM resistive memory, the graph of the current in a voltage rising curve must have a format different from the curve obtained for the curve in a downward tension. An important memory device mechanism is the transition from the high resistance state (HRS) to the low resistance state (LRS) under applied voltage variation. It may be more useful for the device to have a fast switching response in the critical voltage where the transition occurs HRS to LRS.

Eight different devices were fabricated:

- ITO/CuO/GO+%1Fe/CuO/Al
- ITO/GO+%1Ag Al
- ITO/GO+%1Cu/Al
- Al/CuO/GO+%1Ag/CuO/Al
- ITO/GO+%0,1Ag/Al
- ITO/CuO/GO+%0,1Ag/CuO/Al
- ITO/CuO/GO+%1Cu/CuO/Al
- ITO/CuO/GO+%1Ag/CuO/Al

3 Results

For the eight devices produced there were combinations of aluminum and ITO contacts and graphene oxide (GO) doped with a transition metal (iron, copper or silver) with or without copper oxide (CuO) layer. In Fig. 1 electrical characterization of the resistive memories is observed. HP 4140B was used for current as a function of voltage (IxV) measurements.

It is observed that no memory had a similar behavior. The most interesting and common fact to notice in almost all devices is that there is an abrupt transition from LRS to HRS and in the sequence there is an abrupt transition from HRS to LRS forming a sort of “thorn”. It can be noted that there is an abrupt change in current in some tensions, in which Zhang et al. [16], in their work with ITO/ZnO/PCMO/ITO-based RERAMs, associated mobile traps (oxygen vacancies) that were occupied by electrons forming a conducting path, the so-called filament conductor. However, in these voltages where there is occurrence of the “thorn”, the weakest point of the conducting filament is destroyed, and according to the authors of this research, results in an electronic properties change.

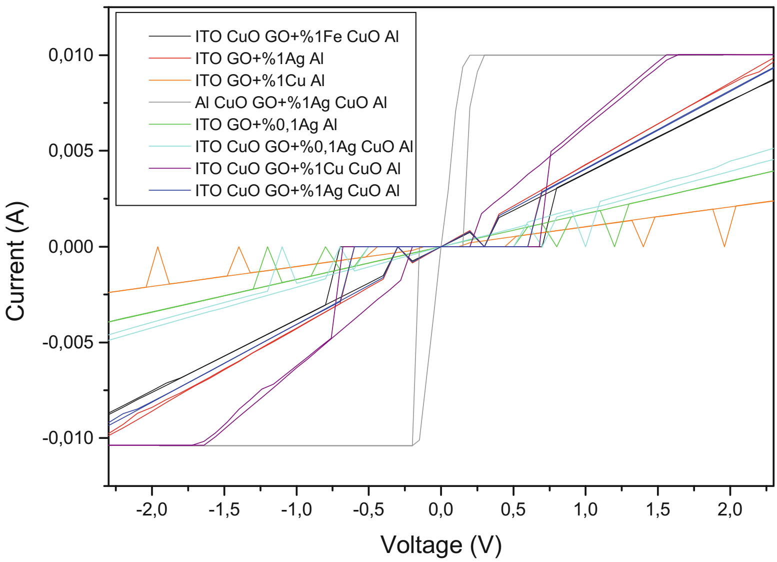
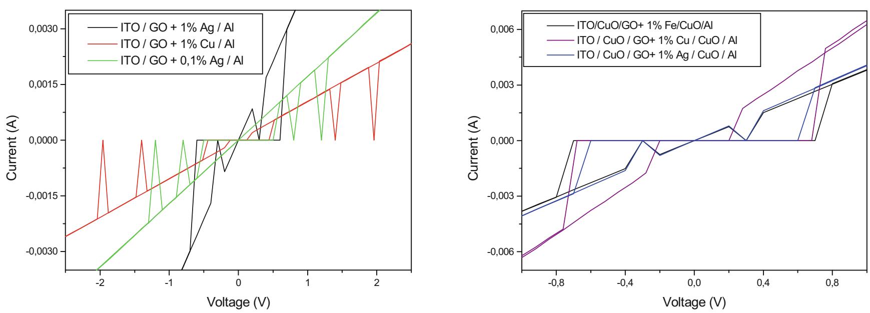


Fig. 1. Current as a function of voltage (IxV) measurements.

In graphs below, some comparisons between similar devices were made. The results were grouped for devices with similar structures.

For Fig. 2a, a three layer structure is shown and for Fig. 2b, a five layer structure interspersed with copper oxide. In the graphs of Figs. 2a and b it is possible to observe that devices have unipolar memory behavior since the SET and RESET occur in the same polarity. For Fig. 2b, it is noted that the SET (HRS for LRS) occurs in values around ±0.7 V to ±0.8 V and RESET occurs between ±0.2 V to ±0.3 V, for the same polarity. Being unipolar, there is no influence of the electric current, thus avoiding the joule effect with heating of device. In addition, the SET and RESET occur in a range less than 0.9 V, which implies a lower power consumption for it to operate.



a b

Fig. 2. (a) Three layer structure and (b) Five layer structure interspersed with copper oxide.

It can be seen that copper interferes in the behavior of devices with respect to the current as a function of the voltage. Such transition metal interferes with the "thorns" formation. When copper (as GO dopant or oxide form) is added in the ReRAM structure, the tendency is for abrupt change in the resistance state to be more difficult to occur. This element probably mitigates effect that possible oxygen vacancies may cause.

In the case of these devices, as they are formed by GO doped with transition metal (iron or copper or silver), filament will be formed as a function of this metal. Eventually mobile traps will be formed, destroying the filament fragile section and resulting in abrupt changes of resistance state ("thorn"). The behavior of filament is seen in Fig. 3.

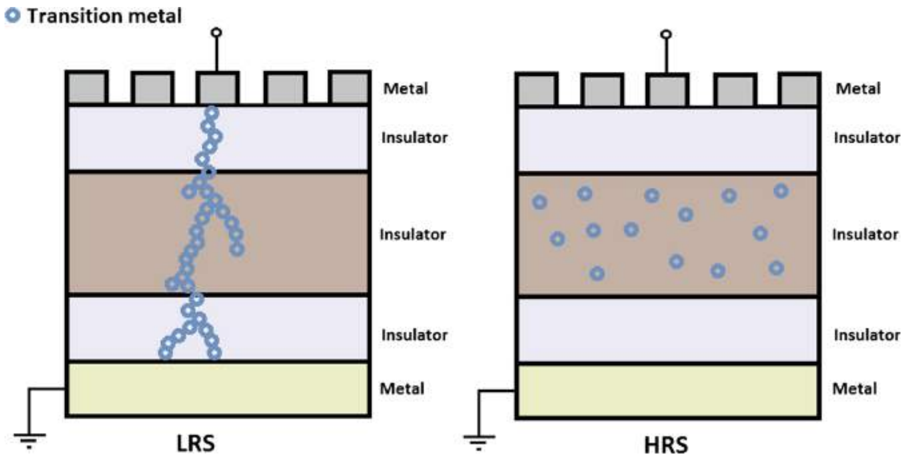


Fig. 3. Behavior of filament.

An interesting fact to note is that the used contacts influence the formation of the filament as well. If the graph for the ReRAM based on the Al/CuO/GO+1%Ag/CuO/Al structure is observed, its behavior diverges from the other devices (Fig. 1).

After the individual characterizations of the devices have been completed, memories with structures in 8×8 matrix format will be fabricated.

Structures will be fabricated in this way (Fig. 4) in order to develop a circuit whose memory stores 64 bits. The high resistance state HRS will correspond to the low level or 0 and the low resistance state LRS will be the high level or 1.

The algorithm for writing will be based on the code for LED matrix operation, which will be associated with the code to obtain resistance at each position of matrix. In this way, a write/read memory array code will be obtained. The program will be uploaded to the Arduino microcontroller which will manage the operations performed by ReRAMs (Fig. 5).

This memory array will be able to save data. It is possible to record and read information dynamically with appropriate algorithm. There is even the possibility of storing images (referring to original idea of LEDs matrix forming images). With these functions, it would be promising to enter the neuromorphic computing area that is one of the ReRAM applications.

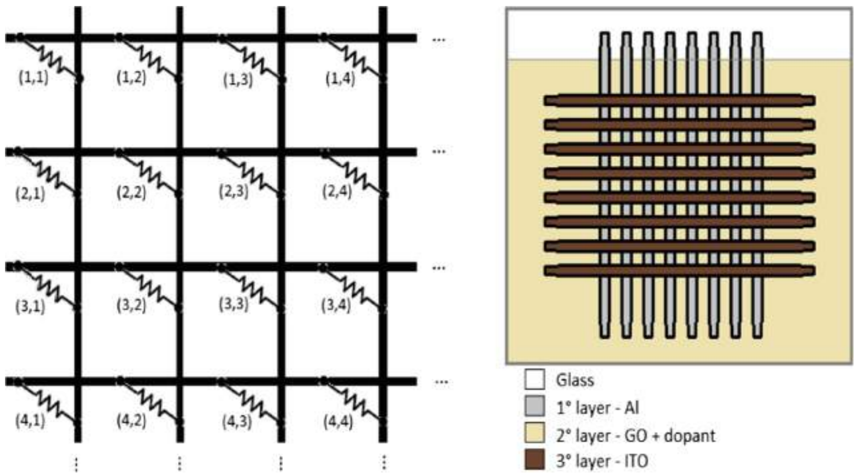


Fig. 4. Memories with structures in 8 × 8 matrix format.

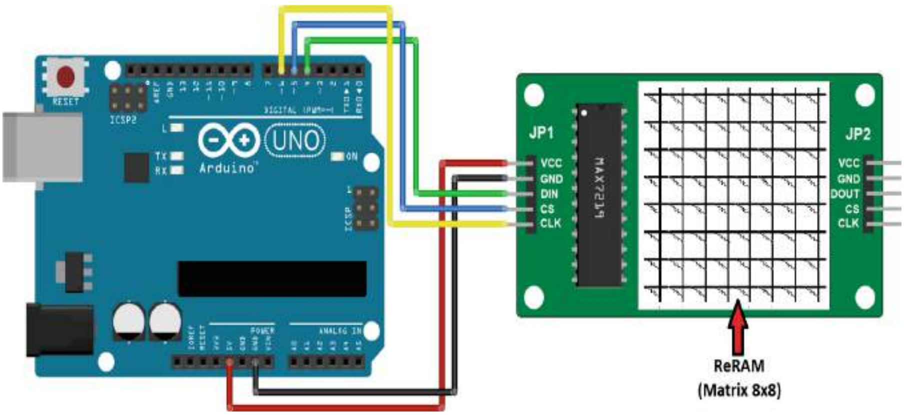


Fig. 5. Arduino microcontroller and ReRAMs.

The basic idea in most ReRAM-based neuromorphic approaches is to consider ReRAM devices, or small ReRAM-based circuits, as artificial synapses. According to Indiveri et al. [17], the idea of using ReRAMs as neural simulators comes from Likharev who introduced the "Crossnets" concept, where memory devices serve as interconnectors corresponding to binary synapses.

Human memory is often associated with ability to retain and use information or acquired knowledge, but there is an important function of being related to learning process. In DeSalvo et al. research [18], she mentions that ReRAM technology advent represents a paradigm shift for artificial neural networks, being the best candidate for emulation of synaptic plasticity and learning mode. Thanks to its non-volatility, high switching behavior and reliability, resistive memories can make the operation of machines close to human brain functioning, including mental processes such as visual recognition and problem solving. It would be a great advance if these devices work with genetic algorithms, which would allow a constant evolution.

4 Conclusion

Eight different devices were fabricated. It is observed that no memory had a similar behavior. The most interesting and common fact to notice in almost all devices is that there is an abrupt transition from LRS to HRS and in the sequence there is an abrupt transition from HRS to LRS forming a sort of "thorn". This behavior can be associated with mobile traps. Copper interferes in the behavior of devices with respect to the current as a function of the voltage. Such transition metal interferes with the "thorns" formation. When copper (as GO dopant or oxide form) is added in the ReRAM structure, the tendency is for abrupt change in the resistance state to be more difficult to occur. This element probably mitigates effect that possible oxygen vacancies may cause.

This memories will be able to save data. It is possible to record and read information dynamically with appropriate algorithm. There is even the possibility of storing images (referring to original idea of LEDs matrix forming images). With these functions, it would be promising to enter the neuromorphic computing area that is one of the ReRAM applications.

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