Graphene oxide resistive memories with threshold switching behavior

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***Abstract*—Resistive random-access memories (ReRAMs) are based on a physical phenomenon called resistive switching (RS). Such a phenomenon occurs when the resistance of a dielectric undergoes changes in response to a strong external electric field. This change can be associated with logical level transition. RS process is reversible and can be reproduced countless times. In this work, the goal is to characterize three different devices and to verify if there is influence of the architecture and contact types. By varying the voltage, electrical current measurements were performed on the memory cells using a picoammeter. Through this analysis it is possible to detect SET and RESET of each device. With the expected performance, the current curves are compared as a function of the voltage. All ReRAM cells have sharp transitions in the SET stage. In the RESET process, devices still show an abrupt transition from low resistance state (LRS) to high resistance state (HRS), which is quite similar to the situation in SET stage. Resistive memory devices present threshold switching. As we have the comparison between the matrix and points structures, there is a probability that the architecture of the cell units can influence due to the electric field.**

***Index Terms*— ReRAM, Resistive Switching, graphene oxide.**

I. Introduction

IN 2008, Hewlett-Packard Company (HP) took an important step forward in advancing beyond CMOS technology, with the construction of resistive memories [1], which were proposed theoretically in 1971 by Leon Chua [2]. ReRAMs are electrical devices based on an insulator thin film between two metal contacts. ReRAMs (resistive random access memory) are currently a solution in the miniaturization of flash memory and the problem of energy consumption. In addition, the use of resistive memories associated with neural networks makes them considered as neuromorphic devices [3].
Resistive memories are devices composed of two contacts, separated by an insulator. These devices have resistivity modified when an external voltage is applied and this process can be repeated several times. The physical phenomenon behind this characteristic is resistive switching [4-7]. This property can be associated with logical level transition, which generates great interest for computer architecture area. These memories have a structure similar to a capacitor (MIM or metal-insulation-metal), which undergoes a resistance transition induced by the application of an electric field. The transition is caused by the formation of conductive filaments within the insulation layer. Filaments may be constituted by ions or oxygen vacancies diffusion.

Basically, there are two types of devices: unipolar and bipolar. Electrical behavior is said to be unipolar when the switching process does not depend on the polarity of the applied voltage. For the case where the SET and RESET happen at different polarities, the behavior is said to be bipolar. The transition from the low resistance state LRS, or logic level 1, to the high resistance state HRS, logic level 0, is known as RESET; on the other hand, the inverse process is called SET.

The goal of this work is to verify the influence of different contacts on the electrical characteristics of the prototyped ReRAMs. By means of this analysis, it is possible to determine the materials most advantageous for the manufacture of these devices, especially by the way in which the current curve may change as a function of voltage. This describes the voltage limits that the system can work on, which is one of the determinants in the energy consumption of the device, as well as its potential heat dissipation capacity. These factors determine the viability of a computational memory unit or a processor in a viable application system. In addition will be made the comparison of two different types of architecture.

II. Experimental

Devices were fabricated on glass substrate (Figure 1). Bottom metal electrode used can be either chrome or copper and top electrode is based on indium tin oxide (ITO). The material chosen for the insulating layer between the contacts was 1% silver doped graphene oxide.

Deposition of top and bottom contacts was made by evaporation. Graphene oxide doped with 1% silver (GO+1%Ag) insulator layer (~ 35 nm) was deposited via dip coating technique. Three devices were obtained: ReRAM Cr/GO+1% Ag/ITO based in matrix structure, ReRAM

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Cr/GO+1% Ag/ITO based in points structure and ReRAM Cu/GO+1% Ag/ITO based in matrix structure.

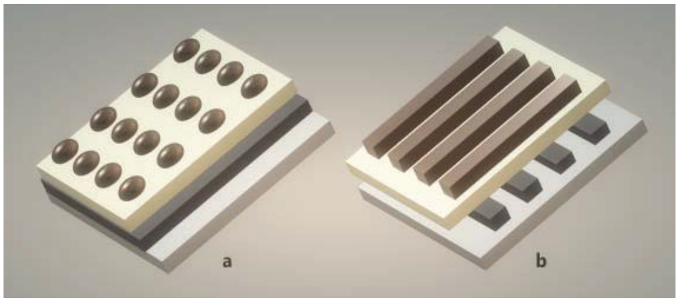

Fig. 1. a) Points and b) matrix structures.

Current and voltage relation was measured by tracer IxV model HP 4140b. In the figure below it is possible to see the arrangement of the device connected through microprobes (figure 2). One of the most important mechanisms of memory device is the transition from HRS to LRS under applied voltage variation, as well as the transition in the inverse path. It may be more useful for device to have a fast switching response at the critical voltage where transition occurs.

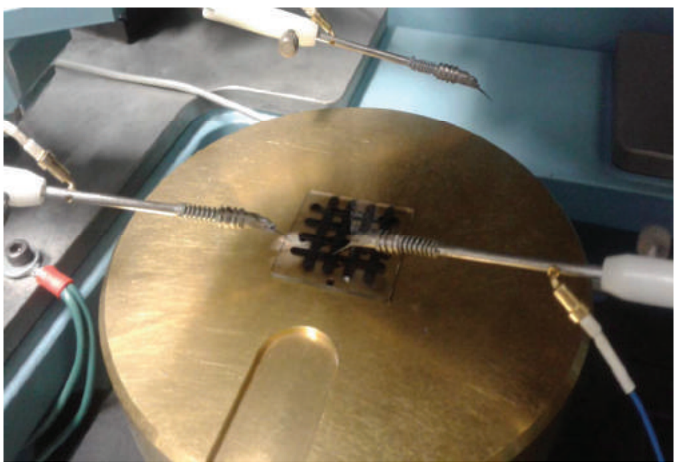

Fig. 2. Arrangement of the device connected through microprobes.

III. Results

Current behavior was measured as a function of the voltage variation (in a range of -2 V to 2 V). Through this analysis it was possible to verify if there are changes of resistivity and, consequently, SET and RESET. In sequence, the curves were compared. Ten cycles of measurements were performed to ensure behavior reproducibility and to verify that the device did not degrade.

To show the influence of different parameters on memories behavior, a comparison between three devices with different architectures (points and matrix) and with different bottom contacts was made.

Resistive memory Cr/GO+1%Ag/ITO based in a matrix is an unipolar type, in which both the SET and RESET operation can be achieved by applying either positive or negative voltage. As can be observed (figure 3), the electric behavior of low resistance and high resistance states is quite different. When the filament is formed (LRS), a connection forms between the electrodes and, therefore, resistance is low. When filament is broken, current flows through the oxide and the system behaves as an insulator.

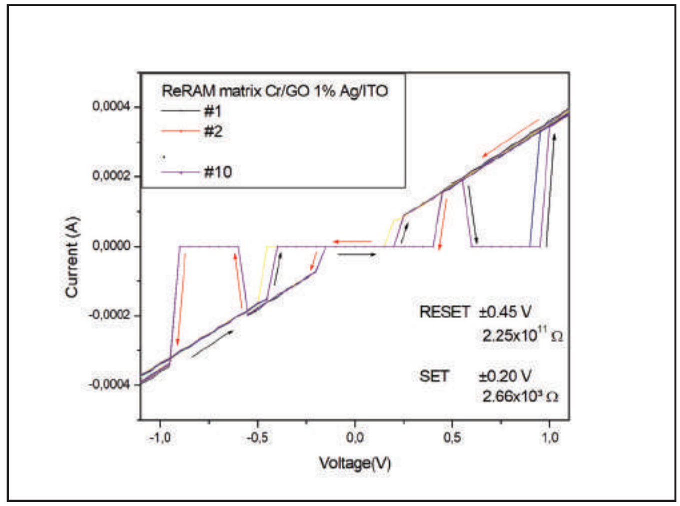

Fig. 3. Typical I-V curves of Cr/GO+1%Ag/ITO matrix structure.

For ReRAM Cr/GO+1% Ag/ITO based in matrix, there are fewer resistive switching processes than point structure. However, the device with copper contacts is the one with fewer occurrences of SETs and RESETs compared to the other two types of memory. Probably the mechanism that influences the formation of conducting filament between electrodes is oxygen vacancy, which occurs in graphene oxide. According to Lee, oxygen vacancies can affect resistive switching in three ways: (I) by grouping and filament formation under influence of an electric field, (II) can control the characteristics of the Schottky barrier, and (III) can form traps for electrons within the Schottky barrier region [4]. In a unipolar device that does not depend on polarity to have its filament formed or destroyed, there is still an influence of the Joule heating effect.

SET and RESET, which require less power to change from one state to another, occur within ± 0.2 V and ± 0.45 V respectively. With a resistance LRS 2.66×10^{3} Ω and HRS 2.25×10^{11} Ω, there is a difference of eight orders of magnitude between states.

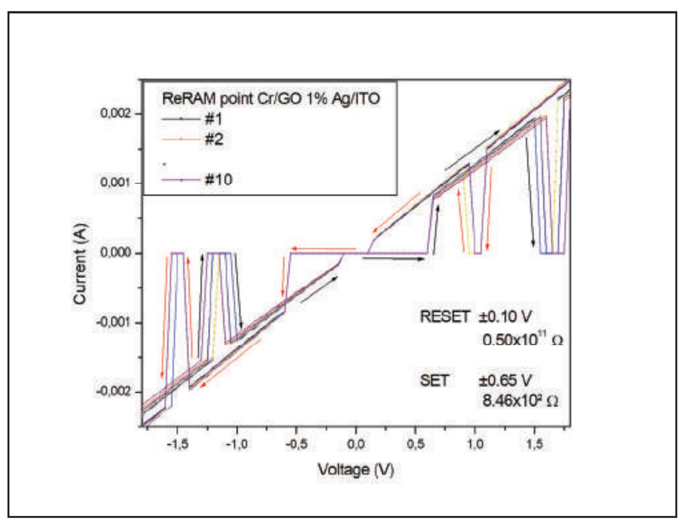

Fig. 4. Typical I-V curves of Cr/GO+1%Ag/ITO points structure.

As we have the comparison between the matrix and points structures, there is a probability that architecture of cell units can influence due to electric field formed when there is a difference of electrical potential between metallic contact and semiconductor contact. As future research, it is expected to perform simulation of electric field behavior in both structures.

Structure of points as top contacts of this device, based on the combination Cr/GO + 1% Ag/ITO, has influence on IxV curve behavior (figure 4). In addition to a greater number of resistive switching processes, the current with which the memory units operate is an order of magnitude larger than the previous device, based on a matrix structure. It is possible to notice that the obtained curve is asymmetric. SET and RESET, which require less power to change from one state to another, occur within ± 0.65 V and ± 0.10 V respectively. With a resistance LRS $8.46x10^2$ Ω and HRS $0.50x10^{11}$ Ω, there is a difference of nine orders of magnitude between states.

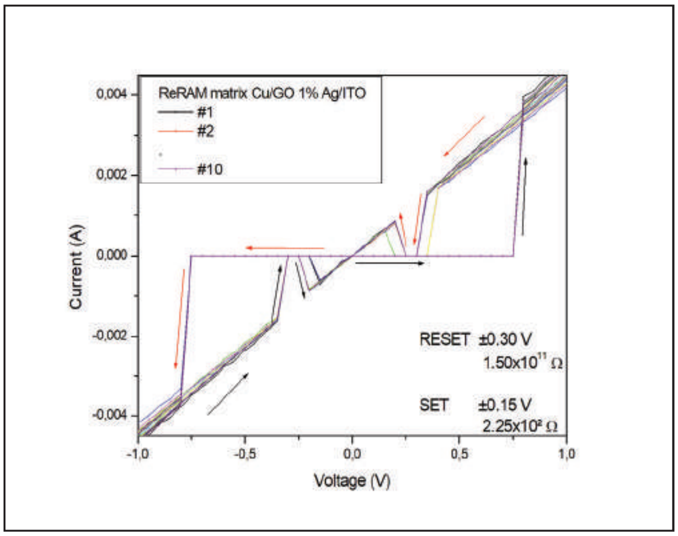

Fig. 5. Typical I-V curves of Cu/GO+1%Ag/ITO matrix structure.

In Fig. 5, it is possible to verify that the last device has a smaller amount of resistive switching processes. Compared with the first analyzed memory, it has an electric current about ten times greater. The RESET and SET, which require less energy in resistive switching process, occur for voltages of ±0.3 V and ±0.2 V respectively. Behavior of the curve near zero voltage is differentiated compared to the other two devices.

All ReRAM cells have sharp transitions in the SET stage. In the RESET process, devices still show an abrupt transition from LRS to HRS, which is quite similar to the situation in SET stage. Resistive memory devices present threshold switching.

In order to compare curves behavior and to verify the current value for each device at a specific point, a voltage of ±1 V was chosen (table I). At this point, we have a low resistance state or logic level 1, which means that there is a filament formed between the contacts. All resistive switching processes happen between -1.8 V and 1.8 V for the three devices, which leads to the fact that these memories require little amount of energy to operate.

TABLE I

DEVICES COMPARISON

Device	-1 V	1 V
Cr/GO+1%Ag/ITO matrix	-3.36E-4 A	3.42E-4 A
Cr/GO+1%Ag/ITO point	-1.12E-3 A	1.12E-3 A
Cu/GO+1%Ag/ITO matrix	-4.44E-3 A	4.78E-3 A

Device behaviors were compared and memory Cr/GO+1%Ag/ITO with matrix structure was taken as reference. In Fig. 6, there is the question of architecture: one device in matrix format and another device containing points. It is possible to note that the current in LRS is lower for the matrix structure device. There is an influence of electric field on the formation of conducting filament and the type of architecture causes changes in electric field.

According to Lee and Pan, crossbar architecture is a new paradigm for memory technology due to its simplicity, performance, robust switching and the possibility of building a dense device [8]. This structure is more advantageous when compared to structure of points because the circuit to make the connections is simpler. Point architecture is a simple capacitor-like MIM (metal-insulator-metal) structure; it is an insulator or semiconductor layer sandwiched by two electrodes [9].

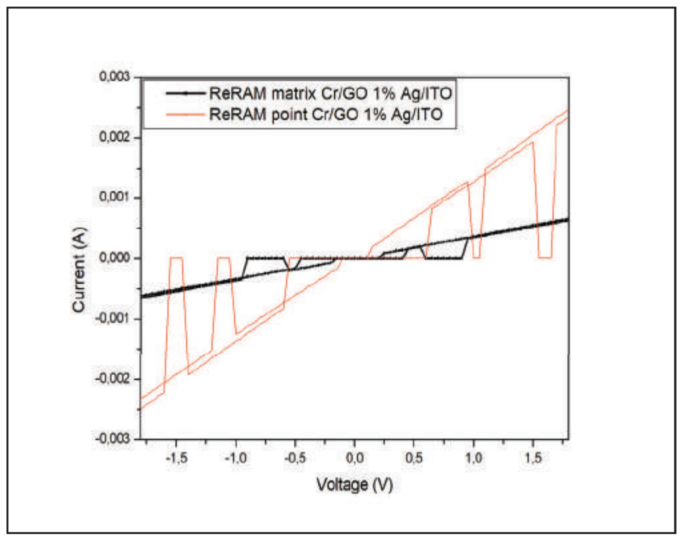

Fig. 6. Comparison between devices with different architectures.

In current versus voltage analysis (figure 7), reference device is compared to the ReRAM Cu/GO + 1% Ag/ITO with matrix structure. The difference in this case is bottom electrode which is composed of a different metal. Other works have reported how copper interferes with filament formation. In his paper, Marinella discusses the formation of the conductive filament and mentions a process called Electrochemical Metallization Bridge (EMB), where memory is the bipolar ReRAM that switches due to cation motion. Generally the reactive electrode can be either silver or copper [7].

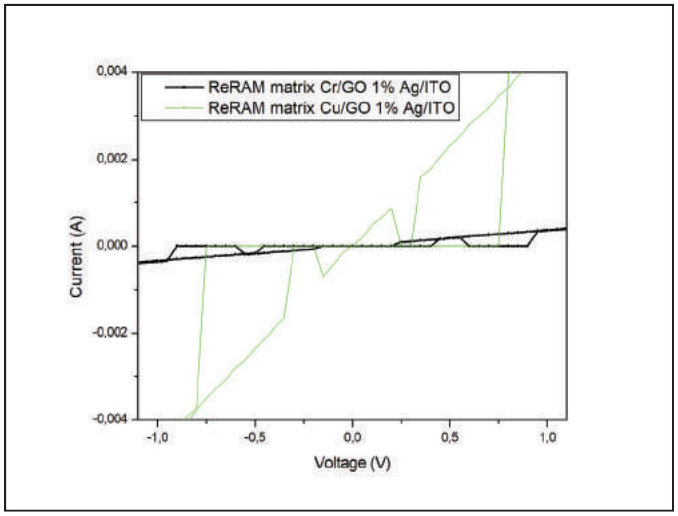

Fig. 7. Comparison between devices with different contacts.

As mentioned earlier, all devices have threshold switching. In Peng and his collaborators research, it is described that substantial Joule heating is generated, which promotes the diffusion of oxygen from indium tin oxide (ITO) into NiO. In fact, in this work, upper contact is ITO and this material has oxygen element as a compound and this may have its contribution. Besides, Peng explains that this diffusion process not only eliminates the oxygen vacancies, but also introduces nickel vacancies in NiO, resulting in weaker conducting filaments and threshold switching [10]. When a parallel is made, there is the possibility that silver (as dopant of graphene oxide) has the same importance as nickel vacancies, which means that it plays a fundamental role in abrupt change of resistance state. Both nickel and silver are transition metals.

Base elements used in neuromorphic computing are devices that simulate behavior of synapses and neurons. What is perceived is that usually memristors are used as synapses because of their simplicity. But few studies have made the use of resistive memories as artificial neurons. Zhang and Kalita present in their research the application of threshold switching phenomenon in artificial neurons. The authors draw attention to one of the main features of the phenomenon, which is the abrupt change from one state of resistance to another. This can be associated with essential properties of the biological neuron: all or nothing spiking, a threshold driven spiking of the action potential, a post-firing refractory period of a neuron and a strength modulated frequency response [11,12].

IV. Conclusion

In this work it was possible to verify the influence of device architecture and the type of metallic material used as contact in the electrical behavior of the resistive memory. Architecture type interferes in the electric field which, in turn, affects the formation or destruction of filament.

In addition, the influence of silver present in the graphene oxide was discussed. Substantial Joule heating is generated, which promotes the diffusion of oxygen from ITO into GO. This diffusion process not only eliminates oxygen vacancies, but also introduces silver vacancies in GO, resulting in weaker conducting filaments and threshold switching.

The specific threshold switching phenomenon, which would be the abrupt transition from a high to low resistance state and vice versa, may be an important feature for applications in neuromorphic architectures. Such peculiarity is desired in this research, because it is expected to obtain the TSM (threshold switching memristor) neuron from memories based on graphene oxide in a future work.

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