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Transmission of wireless neural signals through a 0.18µm CMOS low-power amplifier

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researchers still are not able to produce clinically viable solutions that meet the requirements of long-term operation without the use of wires or batteries. Another problem is neural compatibility with the electrode probes. One of the possible ways of approaching these problems is the use of semiconductor biocompatible materials (silicon carbide) combined with an integrated circuit designed to operate with low power consumption. This paper describes a low-power neural signal amplifier chip, named Cortex, fabricated using 0.18µm CMOS process technology with all electronics integrated in an area of 0.40mm^2. The chip has 4 channels, total power consumption of only 144µW, and is impedance matched to silicon carbide biocompatible electrodes.

I. Introduction

Although research with Brain Machine Interfaces (BMI) has evolved with great speed in recent years, researchers still do not have reliable BMI systems, which has prevented widespread clinical testing and, ultimately, assisting individuals with neurological and physical disabilities.

In order for BMI to effectively make use of the advances in robotic and computer technology, it is vital to find a biological interface that meets the requirements of long-term electrical reliability, low-power operation, and biocompatibility. These requirements are of special importance. First, commonplace systems are based on batteries that eventually discharge and must be replaced after short periods of time, resulting in additional maintenance requirements; Second, many systems rely on materials that may not have reliable biocompatibility, and can possibly erode with time, demanding costly and high-risk replacement procedures [1-2]. In this paper, our contribution focuses on addressing these two issues.

This project describes the development of a wireless BMI system – see Figure 1, with constraints of very low-power consumption and biocompatibility. Our solution relies on two features: (1) we use a chip designed to operate with a power consumption that is small enough for it to be powered by radio frequency antennas, dispensing with the need for batteries; (2) we use a probe manufactured from silicon carbide (SiC), a material that demonstrated excellent neural compatibility with murine mouse brain tissue in vivo [13].

This paper presents the first version of the Cortex chip, which is a 4-channel amplifier that magnifies neural signals to levels high enough for them to be processed by a computer.

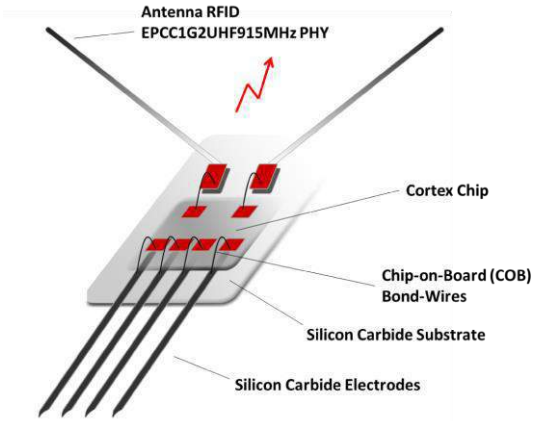


Fig. 1. Conceptual diagram of the proposed BMI system, which integrates the Cortex chip, described in detail in this paper, with cubic silicon carbide electrodes (3C-SiC) and an RFID wireless interface.

II. Concepts and Related Works

A. Gliosis and Neural Implants

The introduction of neural interfaces inside the central nervous system (CNS) inevitably damages the delicate tissue which leads to the neural inflammitory response, gliosis [1–5]. Gliosis is a reactive cellular process concerning physiological changes in glial cells in an effort to restore the blood brain barrier and protect the CNS. However, if a device is recognized as a foreign object by the glia, it can lead to a chronic inflammitory reaction which normally results in the encapsulation of the device by tightly knit scar tissue, also named a glial scar. Glial scar encapsulation has been noted to lead to a reduction in reliability of the implanted devices, and is one of the leading causes preventing their therapeutic use. The search for alternative materials may help aliviate this issue and is currently an active research topic.

Fig. 2. A SiC optrode developed at USF [14]. The optrode features four platnium recording electrodes and an amporphous SiC coated SU-8 wavegude. The electrodes are desingeld to be connected to a neural signaling amplifier at the pads on the right side of the image.

B. *Neural signal amplifiers*

Many neural signal amplifiers have been developed since 2000 [8-11], but none of them meets our proposed needs. In former works, some authors implemented simple Operational Transconductance Amplifiers (OTA's) for neural signal amplification based on older technologies (1500 nm to 500 nm). Modern designs are based on more advanced technologies, such as 0.18 µm CMOS, leading to lower power consumption and die area, which are mandatory characteristics for our project.

Many of the recent designs also have drawbacks. Some authors [11] completely avoid the use of on-chip (and even off-chip) capacitors, to minimize power consumption. This design decision forces them to use DC coupling (instead of AC coupling) at the amplifier input, forcing them to deal with DC component elimination *a posteriori*. This can be an issue because there might be a loss of data due to the circuitry. Other authors simply choose to use very large transistors [8] at the input to reduce flicker noise (which appears at very low frequencies), but this design increases the power consumption, even when using more advanced technologies.

III. The Cortex Chip

A. *Silicon Carbide (3C-SiC) Neural Interface*

In a previous study [13], it was observed that cubic silicon carbide (3C-SiC) is highly compatible with CNS tissue in a murine mouse model. Therefore, in this work, we opted for 3C-SiC as the most adequate material to define a permanent implantable neuronal prosthesis. Figure 2 presents 6 µm thick, 7 mm long 3C-SiC optrode developed in our laboratory with four gold electrodes, an SU-8 optical waveguide, and amorphous SiC insulation. The tab contains 4 bonding pads to connect the electrodes to the proposed electronics.

B. *Design of the Operational Transconductance Amplifier*

An ideal implantable BMI not only includes material neural compatibility but it should also include the following: very low power consumption to operate without batteries, broadband data transmission, small area encapsulation (no off-chip components) and, avoid high power radio frequency operation, below the absorption limits of biological tissues. With these requirements in mind, we designed a special purpose Operational Transconductance Amplifier (OTA), detailed as follows.

Figure 3 shows the chain structure of our amplifier. It has two stages, each with 14.14 of voltage gain, and an output buffer for test purposes. The gain stages gm1 and gm2 are comprised of a fully differential OTA, featuring high open loop gain, low input referred noise, and high power supply rejection ratio (PSRR). Details of the OTA architecture are shown in Fig. 4. The gain per stage is defined by the ratio of the capacitances C2 and C1, leading, in this case, to a value of 23dB. Besides the gain, the capacitors act as high pass (C1) and low pass filters (C2 and C3). These filters are designed to reduce flicker and thermal noise inside the signal band.

Figures 3 and 4 present the architecture used in our Cortex amplifier and the schematic of the developed OTA respectively. Each amplifier stage has a gain of 14.14 V/V. The last stage of the Cortex architecture diagram shows two support buffers enabled only during test measurements with external equipment. It should be noted that the on-chip capacitors are very small (~4pF), which contributes to a significant reduction in power consumption.

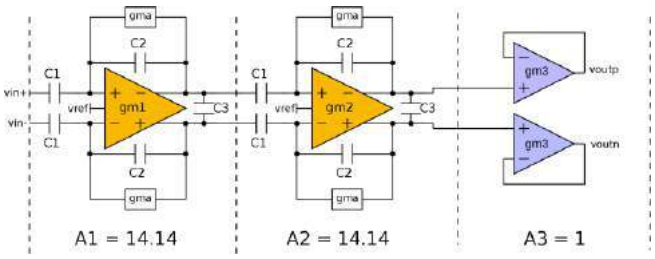


Fig. 3. Regular two-stage OTA architecture with 14.14 V/V gain per stage (~200x total gain of ~46dB).

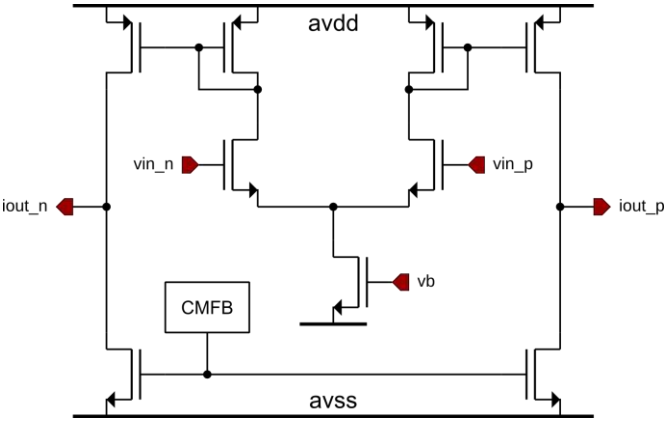


Fig. 4. Schematic of the Operational Transconductance Amplifier (OTA) and Common Mode Feed Back circuit (CMFB) used in each stage of the Cortex chip.

C. *Wireless link*

For the wireless functionality, we opted for an off-the-shelf solution. We chose the 915MHz PHY CM9011ff [12] from Chipus Microelectronics, illustrated in Figure 5; this choice was guided by the fact that its operation, in the range from ~1-3GHz, minimizes the channel loss for edge-to-edge coupling in biological strata.

In this solution, the data stream will be up to 800 kbps with 4 channels using a 10-bit 20kHz ADC; in accordance to the maximum specific absorption rate (1.6W/kg) defined by the Federal Communications Commission (FCC).

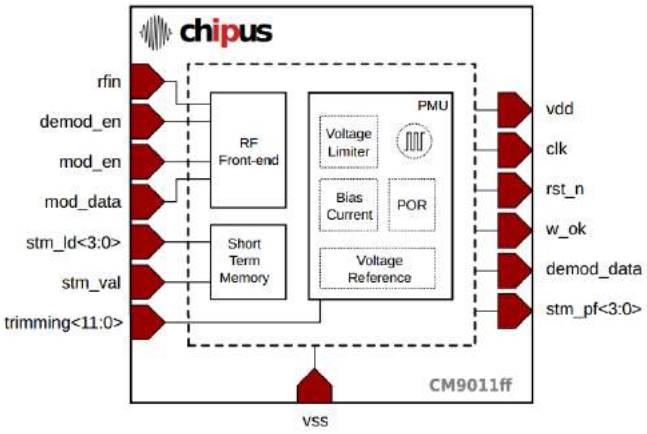


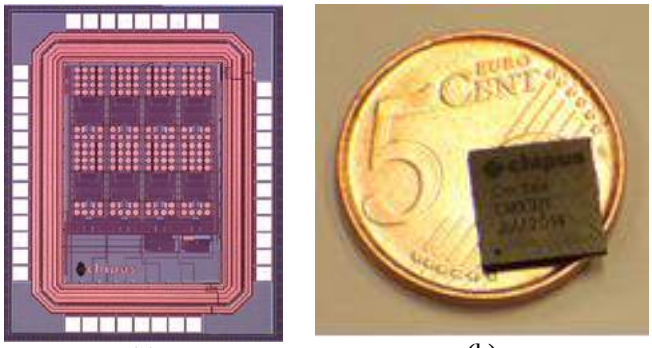
Fig. 5. RFID PHY block diagram from the CM9011ff off-the-shelf chip developed by Chipus Microelectronics. It operates at 915MHz with 1.5µA for passive RFID tags.

IV. Results

In this section, we present the results of functional tests for our integrated circuit. Figure 6a shows a photo of the die manufactured in 0.18um CMOS technology. The core dimensions without pads are X=572um and Y=782um.

The combined die was encapsulated in a QFN64 package, as presented in Figure 6b. Three of the packaged devices have been integrated with silicon carbide electrodes using the chip-on-board (COB) process. They will be implanted in rat brains for *in-vivo* tests in the next stage of development.

In Figure 7 we present the gain, in dB, of our system - while in Figure 8 we present the power supply rejection ratio (PSRR).



(a) (b)

Fig. 6. (a) Cortex die photo (version with internal test pads); and (b) Cortex chip encapsulated in a QFN64 surface mount package for device integration and electrical testings.

We tested th IC with emulated neural signals (1mV and 100µV) which were loaded into a programmable signal generator and injected at the input of the Cortex chip.

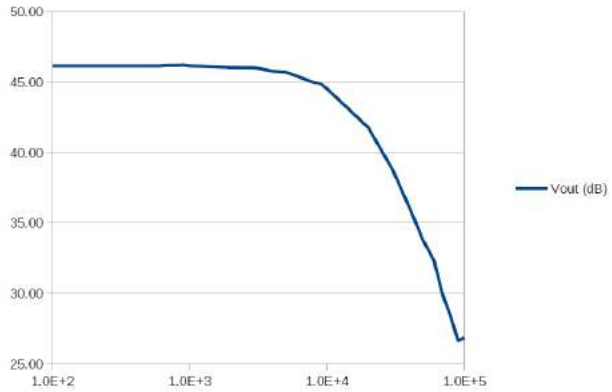


Fig. 7. Measured amplifier frequency response – showing a gain of 46dB (200x) up to 10kHz.

Fig. 8. Measured power supply rejection rate (PSRR) vs frequency – displaying a worst case value of 64dB.

This signal was reproduced with two input amplitudes: 1mV and 100µV. The results of the amplification are shown in Figures 9 and 10. We are particularly interested in both the Local Field Potential (LFP / 5mV) and the Action Potential type (AP / 100uV) neural signals.

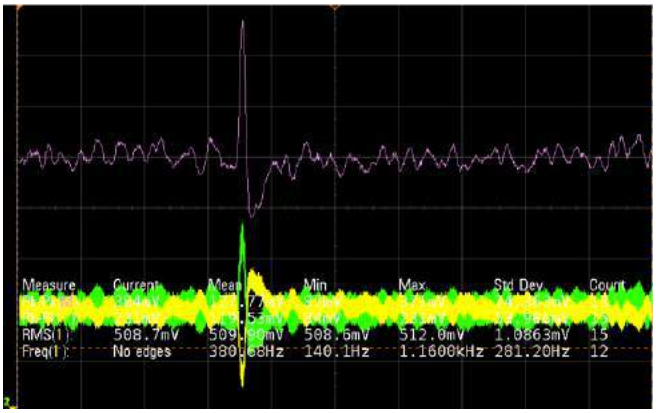


Fig. 9. Measured Cortex amplified output data, using an input signal with 1mV amplitude (typical of LFP neural signals); green and yellow are the differential outputs from the Cortex chip; purple is from the oscilloscope math subtraction operation.

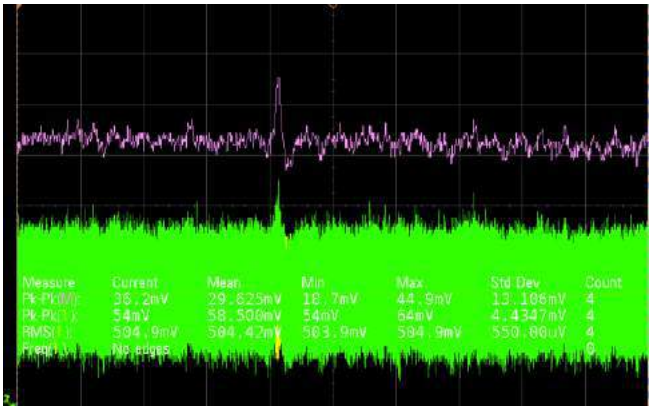


Fig. 10. Measured Cortex amplified output data, using an input signal with 100µV amplitude (typical of AP neural signals); green and yellow are the differential outputs from the Cortex chip; purple is from the oscilloscope math subtraction operation.

Tables I and II present the summary of the results obtained for the Cortex chip in comparison with previously published results for similar circuits. Table II shows that our chip has the following advantages: better PSRR and power consumption performance, smaller area per channel, and AC instead of DC coupling.

V. CONCLUSION

This paper presented the Cortex chip, a low-power neural signal amplifier fabricated in a 0.18µm CMOS process with all electronics integrated into an area of 0.40mm^2. The chip was designed with 4 channels and its total power consumption was only 144µW. It was designed to match the impedance of the SiC electrodes, thus enabling better neural compatibility of the entire system. Furthermore, it is integrated with a RFID PHY for wireless communication. The results showed that LFP/5mV and AP/100µV neural signals can be sampled by the system's probe without distortion. Finally, the Cortex chip power consumption was remarkably low in accordance with the requisites of the project. Our design has demonstrated promising results as an integrated circuit for brain-machine interfacing, demonstrating its potential for in a future brain-controlled device.

TABLE I. SUMMARY OF SYSTEM PERFORMANCE

Regulated Supply Voltage	1.8V typ. (1.6V min. – 2.0V max.)
Regulator PSRR	80dB
Neural Signal Coupling	AC
Neural Signal Amplifier Gain	46dB (0.2 – 10kHz)
Input-Referred Noise	36µVrms (0.2 – 10kHz)
Number of Channels	4
Bandwitdth	0.2kHz-10kHz
Process	Silterra, CMOS 0.18µm
Total Chip Area	0.447mm^2 (0.111mm^2/Ch)
Total Power	144µW (36µW/Ch)

TABLE II. IMPROVED FEATURES

Feature	Other Authors	This Work
Power (per channel)	80µW/Ch [8]	36µW/Ch
Regulator PSRR	5.5dB [9]	64dB
Chip Area (per channel)	0.160mm^2/Ch [10]	0.111mm^2/Ch
Neural Signal Coupling	DC [11]	AC

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SiC for Biomedical Applications

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Keywords: Biotechnology, biosensor, neural interface, glucose

Abstract. Silicon carbide is a well-known wide-band gap semiconductor traditionally used in power electronics and solid-state lighting due to its extremely low intrinsic carrier concentration and high thermal conductivity. What is only recently being discovered is that it possesses excellent compatibility within the biological world. Since publication of the first edition of ***Silicon Carbide Biotechnology: A Biocompatible Semiconductor for Advanced Biomedical Devices and Applications*** five years ago [1], significant progress has been made on numerous research and development fronts. In this paper three very promising developments are briefly highlighted – progress towards the realization of a continuous glucose monitoring system, implantable neural interfaces made from free-standing 3C-SiC, and a custom-made low-power 'wireless capable' four channel neural recording chip for brain-machine interface applications.

Introduction

Cubic silicon carbide (3C-SiC), with a band gap of 2.3 eV, has found applications in the fabrication of micro-electromechanical machine (MEMs) devices, as it can be grown heteroepitaxially on silicon substrates. Our epitaxial growth process on 100 mm Si substrates has previously reported using a hot-wall chemical vapor deposition (CVD) reactor with silane and ethylene precursors [2]. Alternatively, unlike single crystal SiC, the amorphous form of SiC (*a*-SiC) can be deposited at relatively low temperatures, allowing for the coating of polymers and other low-temperature materials [3]. These two forms of SiC (3C and *a*-SiC) are ideal for use in biomedical devices as they encompass a cost-effective processing approach, allowing for the synthesis of thin films in conjunction with cost effective materials, like silicon and polymers. This approach avoids the need to etch away expensive bulk hexagonal SiC substrates to construct micron sized, freestanding devices. In this paper, we will not only detail the development of 3C-SiC and *a*-SiC for biomedical devices, but will specifically discuss the development of SiC-based continuous glucose monitoring and implantable neural interface devices. This research is motivated by the fact that SiC possesses an extremely high level of biocompatibility, which is an extremely critical requirement for long-term implantable biomedical devices [1].

One way to produce a "smart" device is to fabricate it using electrical components that allow for the control of current flow. Semiconductor materials are the backbone of these types of electronic devices, with silicon (Si) being the mainstay material of choice due to a myriad of fabrication techniques. However, Si has proven to have low levels of bio- and hemocompatibility, and therefore long-term implantable technology based on this material has displayed variable performance reliability [4].

In this paper, we are exploiting the combination of physical, chemical, and biological properties of SiC to develop a family of biomedical devices. Our "smart" biomedical devices are designed around 3C-SiC in combination with *a*-SiC insulation. The latter material possesses a high dielectric

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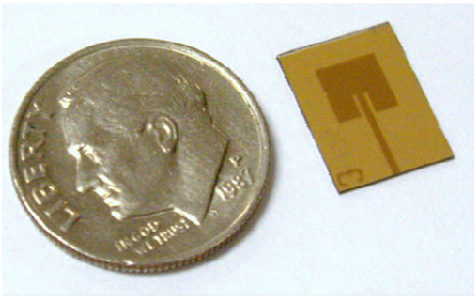
In this paper, we are exploiting the combination of physical, chemical, and biological properties of SiC to develop a family of biomedical devices. Our "smart" biomedical devices are designed around 3C-SiC in combination with *a*-SiC insulation. The latter material possesses a high dielectric

K value, potentially not only enabling it to act as an excellent insulating coating but also as a hermetic casing for delicate silicon electronics. 3C-SiC has shown excellent *in vivo* biocompatibility across multiple animal species [5, 6], and *a*-SiC, which has also shown excellent biocompatibility, performed well in clinical trials involving blood stents [7]. In the next sections, we discuss two of our device applications; a continuous glucose monitor and implantable neural interfaces.

SiC Biomedical Devices

Continuous Glucose Monitoring. The first device, which has been demonstrated *in vitro,* is a continuous glucose sensor employing a shift in RF frequency as a function of blood glucose level (Fig. 1(a)) [6]. The change in glucose level manifests itself electrically as a change in the electrical permittivity of the blood. To test the sensor as a function of glucose level, measurements were performed using synthetic body fluid (SBF), which is electrically equivalent to blood plasma, and pig blood; the result observed was a clinically useful change in frequency (See Fig. 1(b)).



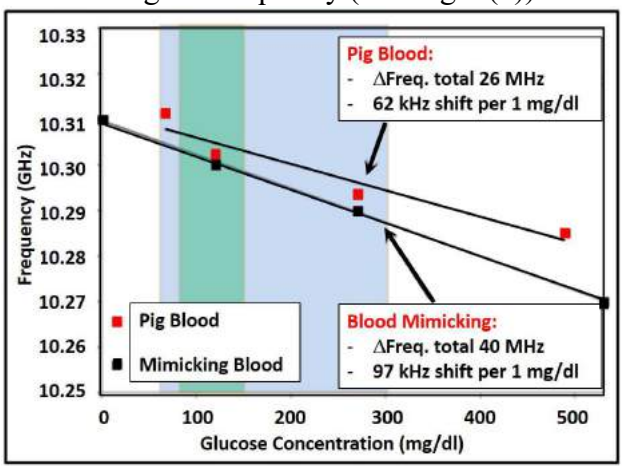


Figure 1. (a) USF continuous glucose sensing SiC antenna comprised of semi-insulating 4H-SiC and a Ti/Au metal patch radiator. (b) 4H-SiC sensor performance showing measurement of blood glucose levels with both synthetic and pig blood. Shaded area normal human glucose range; non-diabetic patient glucose range shown in dark blue (center color band) for reference.

It should be noted that there is still some work to be done to make the device clinically viable. The glucose measurements were performed at 10 GHz, which is a RF band not normally used for biomedical devices. In addition it requires an active, or powered sensor to be powered *in vivo*, which presents many challenges associated with incorporating a power source, such as thermal heating issues, etc. As a consequence, new research at USF is seeking to exploit the ability to remotely sense blood glucose level using a passive RFID type of approach. In short, RF frequency electromagnetic waves are transmitted to a passive antenna implanted *in vivo*. Figure 2 shows the system configuration for this passive sensor strategy, although more thorough and controlled experiments are needed to confirm the repeatability and reliability of the preliminary observations. The patch antenna for this configuration was redesigned for operations in the ISM band (2.45 GHz center band), changing its dimensions from 11.5 mm x 8.5 mm x 0.37 mm to 2 61 mm x 46 mm x 1.27 mm. Clinically relevant levels of glucose were loaded into a blood mimicking solution, which lead to changes in the transmitted wave amplitude, leading S_{21} amplitude measurements which are linked directly to glucose level (see Fig. 2). These measurements, for cost and ease of fabrication purposes, were made using standard copper RF boards, and we are currently fabricating a semi-insulating 4H-SiC antenna to serve as the passive implanted sensor.

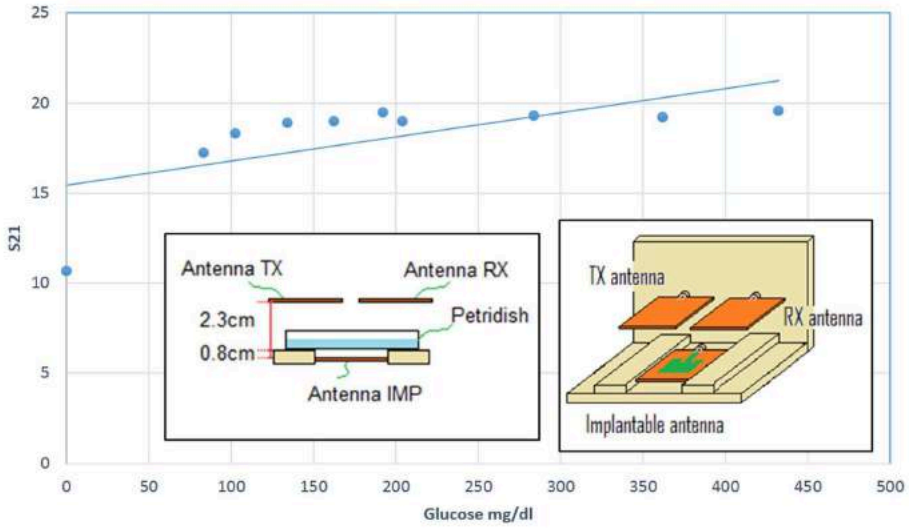


Figure 2. Preliminary ISM band remote read CGM sensing system data. Insets cross section of experimental setup and 3D view, respectively. Note useful glucose detection up to ~200 mg/dl.

Implantable Neural Interfaces. Neuronal devices show an array of problems after implantation into the central nervous system, most of which manifest as decreases in reliability or even complete device failures [8, 9]. One hallmark of this problem is displayed in a chronic inflammatory response which leads to local neural degeneration. Our second presented device works to counter this issue through the use of the 3C-SiC platform. We have previously shown that these passive devices have demonstrated excellent physical robustness as well as surprising flexibility [10] (See Fig. 3), and 3C-SiC has not displayed measurable chronic inflammatory issues *in vivo* [5].

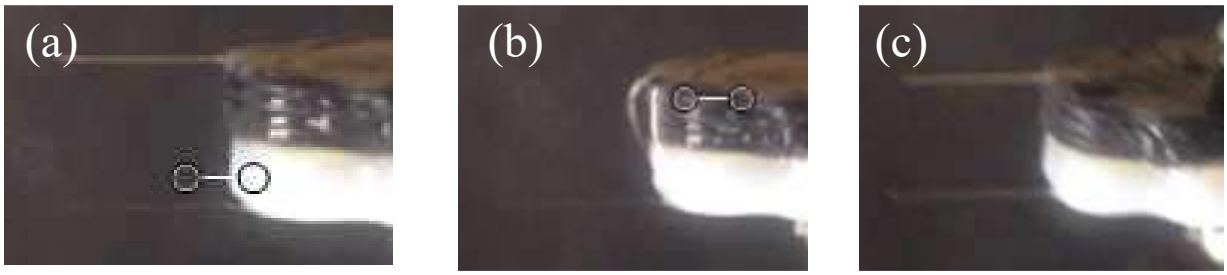
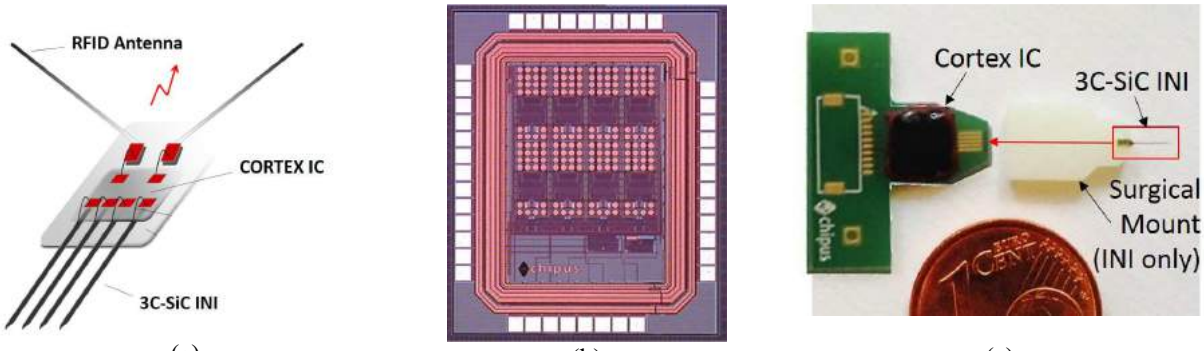


Figure 3. A 3C-SiC probe (on black ABS backing) compared with a similar Si probe (on white ABS plastic). Probes approximately 5 mm long, 80 µm wide and 15 µm thick (a) Prior to immersion in PBS, (b) directly after immersion, showing 3C-SiC probe bent ~90°. (c) After liquid evaporation, 3C-SiC returns to original shape. Action repeatable without fracture or degradation.

Wireless-Capable BMI Recording IC. Brain machine interfaces (BMI) using implantable neural interfaces have yet to produce clinically viable solutions meeting both of the requirements of long-term operation while not using external connecting wires or implanted batteries. One possible solution is to integrate our SiC implantable neural implant and combine it with wireless enabled, low power consumption integrated circuits. Fig. 4 shows one such low-power neural signal amplifier chip, named Cortex, fabricated using 0.18µm CMOS process technology integrated in an area of 0.40 mm^2 [11]. The chip has 4 channels, total power consumption of only 144µW, and is impedance matched to our SiC implantable neural interface electrodes.

The Cortex IC was desgined to have very low power consumption to operate without batteries, possess small area encapsulation with no off-chip components, include the ability to interface with broadband data transmission, and have low power radio frequency operation below the absorption limits of biological tissue. The amplifier has two stages, each with 14.14 V/V gain, and an output buffer for test purposes. The gain stages, noted as gm1 and gm2, are comprised of fully differential

operational transconductance amplifiers, featuring high open loop gain, low input referred noise, and high power supply rejection ratio (PSRR).



(a) (b) (c)

Fig. 4. (a) Conceptual diagram of proposed BMI system, which integrates the 4 channel Cortex integrated circuit (IC) chip directly on a 3C-SiC implantable neural interface (INI) and an RFID wireless interface. (b) Cortex die photo and (c) Photograph of Cortex IC packaged on a neural probe PCB interface with a 3C-SiC INI (not yet intetegrated into package) shown for reference.

A wireless off-the-shelf solution was incorporated for the Cortex chip. We chose the 915 MHz PHY CM9011ff from Chipus Microelectronics [12] since its operation minimizes the channel loss for edge-to-edge coupling in biological strata. The 4 channel speed is up to 800 kbps, using a 10-bit, 20kHz analog to digital conversion, in accordance to the max specific absorption rate (1.6W/kg) defined by the Federal Communications Commission. Summary of the results for the Cortex chip in comparison with published results for similar circuits may be found in [11], where it is shown that our chip has the following advantages: better PSRR and power consumption performance; smaller area per channel; AC instead of DC coupling compared with off-the-shelf chips.

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